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RESEARCH PAPER

Breaking the limits of virtual reality display resolution: the advancements of a 2117-pixels per inch 4K virtual reality liquid crystal display

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ABSTRACT. This work presents a breakthrough in the development of high-resolution virtual reality (VR) displays of 2117-pixels per inch (PPI) liquid crystal displays (LCDs). This technology significantly improves the dynamic range and reduces the screen door effect in VR displays. The challenges and potential solutions for achieving over 2000-PPI LCDs, including the design of the aperture ratio of pixels, improvements in LC efficiency, and overall transmittance, are discussed. Moreover, the use of mini-light-emitting diode backlight and low-power solutions to maintain the image quality in high-resolution designs are also proposed.

Keywords: virtual reality; liquid crystal display; display; high resolution; sub-pixel rendering; mini-light-emitting diode backlight; high dynamic range

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1 Introduction

The demand for higher display quality in virtual reality (VR) displays has increased in recent years, leading to continuous improvements in specifications such as resolution, color gamut, and response speed.[1–3] To reduce the screen door effect, VR display resolution has been raised from 500 to 600 pixels per inch (PPI) in 2017 to over 2000 PPI.[4,5] The "screen door effect" in VR is a visual artifact in which the user perceives a grid-like pattern, resembling a screen door, caused by noticeable gaps between pixels or subpixels on the VR display. It can reduce the immersion and visual quality of VR experiences. However, the highest resolution that can be mass-produced in the market is currently around 1200 PPI.[6]

To meet the demand for higher PPI displays, we propose the first 4K VR LCD technology exceeding 2000 PPI. Although many micro organic light-emitting diode (OLED) displays with higher PPI numbers (3000 to 5000 PPI) based on semiconductor chips have appeared on the market,[7] their panel sizes are relatively small. The enlargement of these panels using an opto-mechanical system may result in a relatively small number of pixels per degree (PPD) that can be seen by the human eye. The PPD specification on the market is currently around 20. In addition, increasing the optical power of a lens also increases its aberration. As a result, we chose to increase the panel size and resolution as an alternative solution.

By contrast, we propose a 2117 PPI 4K VR LCD with a higher PPD specification of ~40, offering better image quality and less image distortion due to the moderate panel size. Additionally, VR LCD with a high partition mini LED backlight improves the contrast, color, and viewing angle, providing a high-quality experience comparable to micro OLED.

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This paper discusses the challenges associated with high-resolution VR LCDs, including the design and specifications of LCDs above 1000 PPI, which differ significantly from traditional mobile phones. Such high-resolution displays require various designs to increase the aperture ratio of pixels while improving the liquid crystal (LC) efficiency and increasing the overall transmittance. Moreover, we propose methods to reduce the panel power consumption and improve the backlight efficiency, aiming to maintain the image quality in designs >2000 PPI while providing customers with lower power components.

2 Architecture and Design

2.1 Achieving High-Resolution VR with Process Limitations

LC displays (LCDs) comprise a layered structure consisting of two polarized panels enclosing a layer of LC solution. Thin glass substrates with alignment layers sandwich the LCs, ensuring their correct orientation. Color filters, often employed in color LCDs, determine the RGB color composition of pixels. A backlight source positioned behind the panels illuminates the LCs, while thin-film transistors (TFTs) or similar electronic components individually control each pixel's voltage, enabling precise manipulation of the LC behavior to regulate the pixel brightness and color. An electronic controller and driver circuitry interpret input signals and drive the transistors to create the desired images, making LCD technology indispensable in modern displays, such as in monitors, TVs, and mobile devices.

As the pixel density increases beyond 2000 PPI, the challenges of fabricating lines and spaces using conventional microlithography equipment become more difficult. For example, in a 2117 PPI striped RGB display, the sub-pixel size is 4.0 μm × 12.0 μm, with a line/space width of ~1 μm. However, the process capabilities of current microlithography equipment may not be sufficient to achieve such a fine resolution. To address this issue, we have implemented a sub-pixel rendering design and algorithm that increases the size of the sub-pixels to 6.0 μm × 12.0 μm, as shown in Fig. 1. When comparing Figs. 1(a) and 1(b), it is evident that Fig. 1(b) has a larger pixel spacing in the horizontal direction (width/space = 1.5/1.65). Consequently, in the horizontal dimension, the original components can have a wider width and spacing, thus exceeding the production limit of 1 μm linewidth and line spacing. By doing so, we are able to realize the required line/space width and produce ultra-high resolution 2117 PPI LCDs

2.2 Thin-Film Transistor Design Improves Aperture Ratio

The aperture ratio is an important specification for LCDs as it impacts the display's brightness. As pixel density increases, the aperture size decreases significantly due to the large size of conventional TFTs used in LCDs. For instance, in a 2117 PPI display, the TFTs used would occupy most of the pixel area, resulting in a very small aperture. To address this issue, we developed a TFT with a smaller size through an optimized design and fine-tuned process. The 2117 PPI pixel equipped with this new TFT maintains a comparable aperture ratio, while also maintaining proper characteristics and reliability. Figures 2(a) and 2(b) demonstrate the impact of different

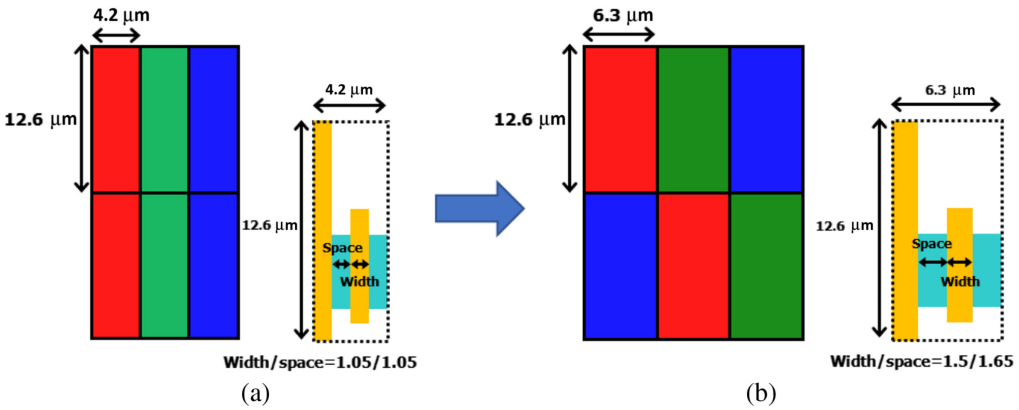

Fig. 1 (a) Striped RGB line/space width reached limit and (b) sub-pixel rendering design with a larger line/space width.

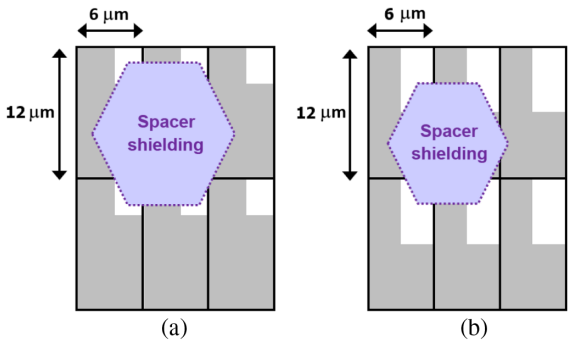

Fig. 2 (a) Conventional TFT device and (b) novel TFT device with a higher pixel aperture ratio.

sizes of TFT devices on the pixel's aperture ratio. Figure 2(b) shows the use of a new TFT design, which results in an aperture ratio of ~19%, more than twice the traditional Fig. 2(a), which has an aperture ratio of only 9%.

2.3 Improve the Efficiency within the Small Pixel

Our new concept of special indium tin oxide (ITO) electrode profile and topography design improves the electric field in the non-aperture area, resulting in a better alignment of the LCs. This leads to an increase in LC efficiency by 70%, as well as an improvement in brightness and contrast by the same amount. Figures 3(a) and 3(b) illustrate the differences between the traditional and new ITO electrode designs, respectively.

Figure 3(a) shows that the effectiveness of the LC decreases if its disclination line enters the aperture area. The design of the ITO electrode and the terrain around the aperture area affect the distribution of the disclination line. The main factor is the PLN via, which bridges the Pixel ITO electrodes and causes an uneven electric field distribution leading to the formation of disclination lines. PLN is an organic material used to planarize the terrain in TFT manufacturing processes. The distribution of dark lines is affected by the relative position between the end of the common (COM) ITO slit and the PLN via. The COM electrode is an electrode used as a reference voltage in circuits. It is typically connected to ground potential and hence it known as the ground electrode. The end of the slit can be placed at the bottom of the via to improve the LC efficiency, but the deep PLN via during the process may not expose the ITO well. Directly filling the PLN via can extend the ITO slit downward, but it is a complicated process. The crab leg design at the end of the slit fine-tunes the position of the dark lines and reduces the impact of process variation. To get better transmittance, we must consider the impact of the PLN via and the ITO electrode design on the distribution of LC disclination lines.

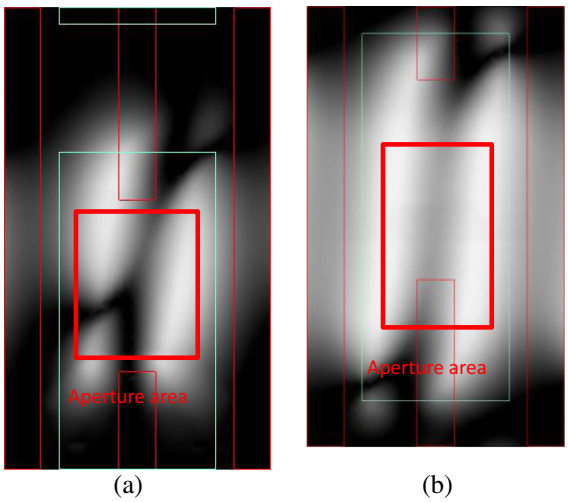

Fig. 3 (a) Conventional pixel design and (b) special ITO electrode profile and topography design.

2.4 Chroma Angular Uniformity

Misalignment between the TFT and color filter (CF) substrate can cause a noticeable color shift when viewed from large angles, especially in high PPI pixels. In general, there is a 1 to 3 μm misalignment between the upper and lower substrates of an LCD. The larger the misalignment is, the more significant the degree of color shift tends to be. To address this issue, it is necessary to enhance the design of the light shielding layer (M1), which can effectively improve this phenomenon. Figure 4(a) shows the situation without metal shielding, and green light leakage can be observed at a wide viewing angle, resulting in color deviation. Figure 4(b) incorporates a layer of M1 as an optical shield, which effectively eliminates color deviations at wide viewing angles.

2.5 Low Power Solutions

As a result of the increased pixel density in high-resolution panels, the power consumption of the panel driving significantly increases, making it impractical for use in wearable devices. The data demultiplexer, also known as the H-driver, accounts for a significant portion of power loss. In this section, we explain methods for reducing power consumption in the H-driver. To address this issue, we implemented a dual-voltage H-driver/V-driver design, which allows for the selection of an appropriate operating voltage based on the specific requirements of the driving circuit. The term "V-driver" refers to the gate on-panel design in TFT technology. This approach effectively reduces the panel driving power consumption and enhances the mass production capabilities. Figure 5(a) illustrates the traditional approach in which both the V and H drivers are powered with a single voltage, leading to excessive power consumption in the H-driver. By contrast, Fig. 5(b) uses different voltage drivers based on varying voltage requirements, resulting in power savings.

The driving frequency of H-driver increases dramatically as the LCD resolution rises to 4K by 4K. Not only does the panel consume more power, but it has worse reliability due to overheated devices. To solve this issue, we adopted low-power driving technology, halving the driving frequency of the H-driver and display signals. In consequence, a more dependable and

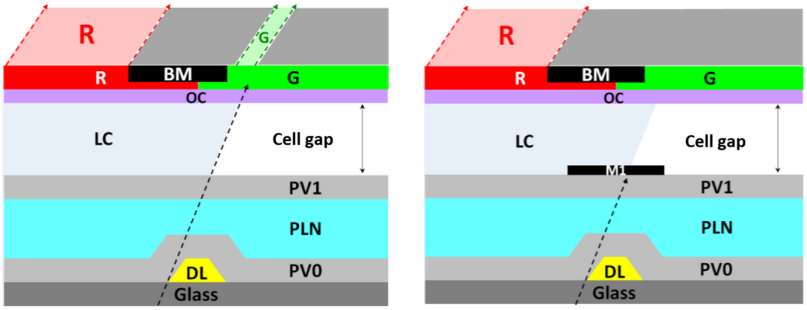

Fig. 4 (a) Without metal shielding and (b) with metal shielding.

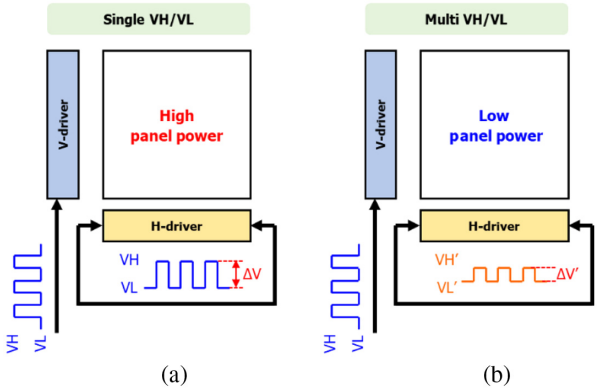

Fig. 5 (a) Traditional approach with signal VH/VL and (b) new approach with multi VH/VL.

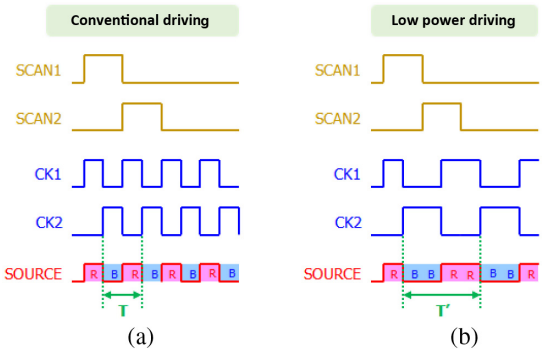

Fig. 6 (a) Conventional driving and (b) low-power driving.

energy-efficient panel is well achieved. By comparing Figs. 6(a) and 6(b), it is evident that the driving mechanism in Fig. 6(b) has a lower operating frequency, leading to a 50% decrease in the operating frequency of the V-driver and a consequent reduction in power consumption.

Heavier parasitic capacitance, which comes from the compact circuit design because the available circuit area is confined by the high PPI display, results in poor driving capability and high-power consumption. The most power consumption occurs in the loading of the H-driver. To overcome this challenge, we implemented several low load designs, such as metal replacement and control line sharing. Both designs are able to reduce parasitic capacitance effectively; therefore, the 2117 PPI VR display can reach a high refresh rate without much energy consumption. Figure 7(a) utilizes the metal replacement method to select a low-load wiring configuration that reduces impedance. Figure 7(b) adopts the control line sharing method to lower impedance. Both of these methods effectively reduce the load and were implemented in our displays.

2.6 High Dynamic Range Mini-LED Backlight

2.6.1 *Improvement of light leakage*

To achieve high dynamic range (HDR) in LCD displays with mini-LED backlights, it is necessary to have a wide color gamut for accurate reproduction of the real world in high PPI VR head-mounted displays (HMDs). In this study, we used a 2117 PPI VR display as the evaluation subject. As shown in Fig. 8, the color gamut of the VR display only reaches 89% of DCI-P3 due to an insufficient width in the red and green areas.

The spectrum of each pure color channel (red, green, and blue) for the LC display (LCD) is shown in Fig. 9. It is evident that red and green pure colors leak light in the blue band, which impacts the performance of these pure colors.

Through careful consideration of the LCD panel, we were able to simulate and adjust the intensity of the red and green pure color leakage light in the blu-ray band to an appropriate level.

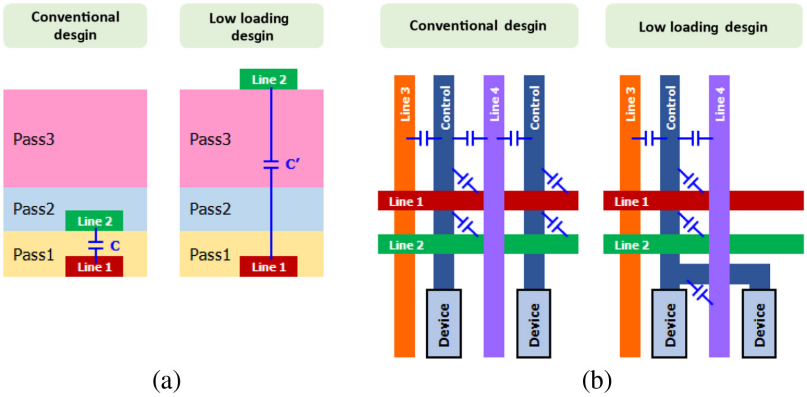

Fig. 7 (a) Metal replacement method for lower capacitance and (b) control line sharing method to avoid the metal crossing.

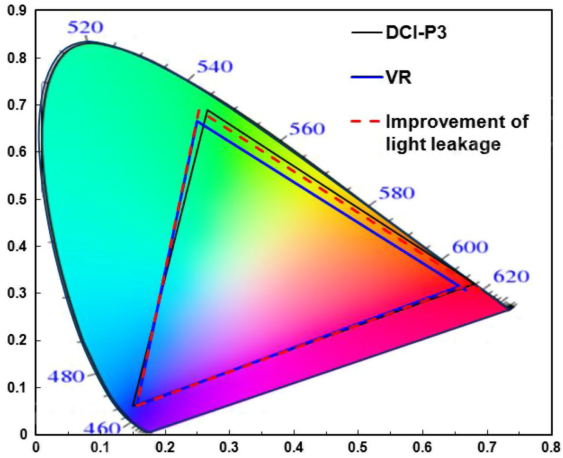

Fig. 8 Color gamut of the VR display with mini-LED backlight.

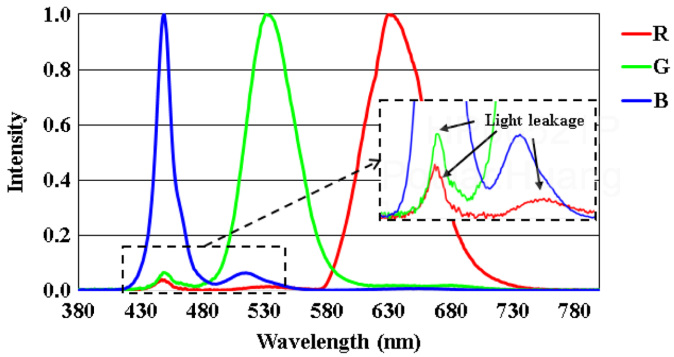

Fig. 9 Spectrum of each pure color channel (red, green, and blue) for the LCD display.

As seen in Fig. 9, the light leakage was greatly improved in the red and green areas, resulting in a color gamut that can exceed DCI-P3 97%, as shown in Table 1. Building on this phenomenon, we utilized high color gamut RGB color resistance with an optimized fabrication process in our new 2117 PPI VR HMD. Additionally, our mini LED backlight is equipped with a quantum dot (QD) film to increase light conversion efficiency and expand the red and green areas, thereby achieving an even higher DCI-P3 color gamut.

2.6.2 *High efficiency backlight with Mini LED + QD*

The efficiency of direct-lit backlight with a mini LED and QD is optimized through properly matched spectrums of mini LED, QD, and color filter. Compared with general edge-lit backlight, the mini LED backlight has narrower full width at half maximum (FWHM) in each color, indicating a better color purity and higher transmittance that meets the National Television System Committee (NTSC) standard, as shown in Fig. 10. NTSC is a color television standard primarily

Table 1 Color gamut before and after light leakage improvement.

Improvement of light leakage	DCI-P3 (%)
Before	89
After	97

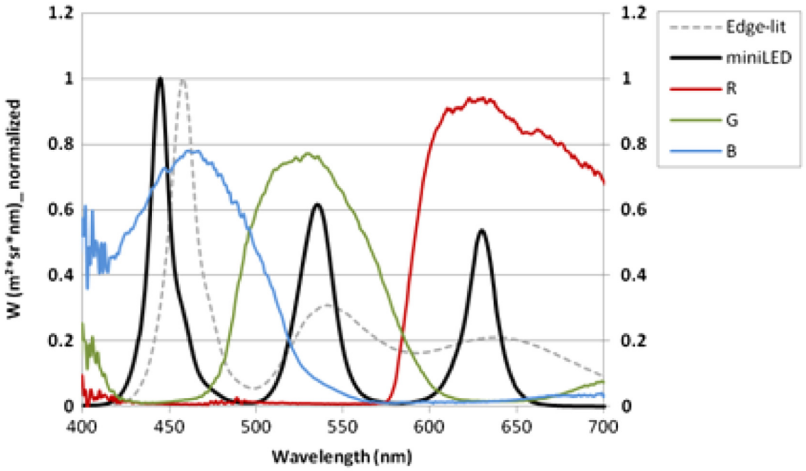

Fig. 10 Spectrum comparison between mini LED + QD and edge-lit backlight.

used in North America and a few other regions that defines the color encoding system for analog television broadcasts and displays.

The black and gray lines in the Fig. 10 compare the spectra of mini LED + QD and edge-lit backlight. R, G, and B respectively represent the three-color spectrum of the color filter. It can be observed that mini LED + QD performs better in the green and red light spectra with narrower FWHM and higher light conversion efficiency. When combined with the color filter's spectrum, it achieves a wider color gamut and purer chromaticity.

2.6.3 *High dimming zones*

Another important point in getting the HDR is the number of dimming zones. In our VR mini-LED backlight device, a single LED driver IC is used with 1024 dimming zones. As shown in Fig. 11, it brings more fine details at the intersection between light and dark. This result can make the brightness and darkness of the image more obvious, thereby enhancing the contrast of the image and making the image quality better.

2.7 Ultra-Thin Backlight

In practical applications, the design of the weight and thinness of VR devices is a crucial aspect that must be considered. In this regard, our VR mini-LED backlight utilizes special optical structure films with a zero OD design to achieve light mixing. The thickness of the backlight module can be controlled below 0.9 mm. The backlight structure is shown in Fig. 12.

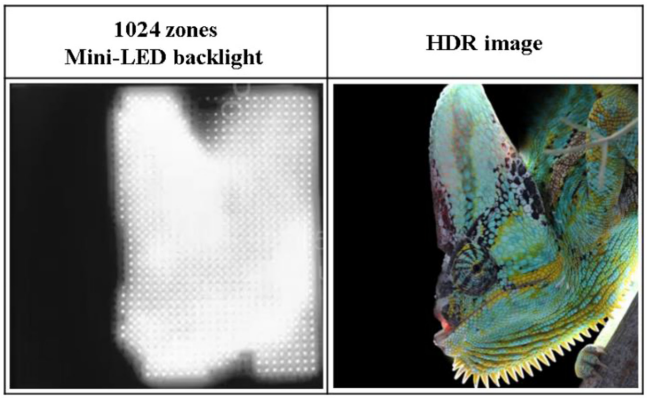

Fig. 11 VR mini-LED backlight with 1024 dimming zones can bring more fine details at the intersection between light and dark.

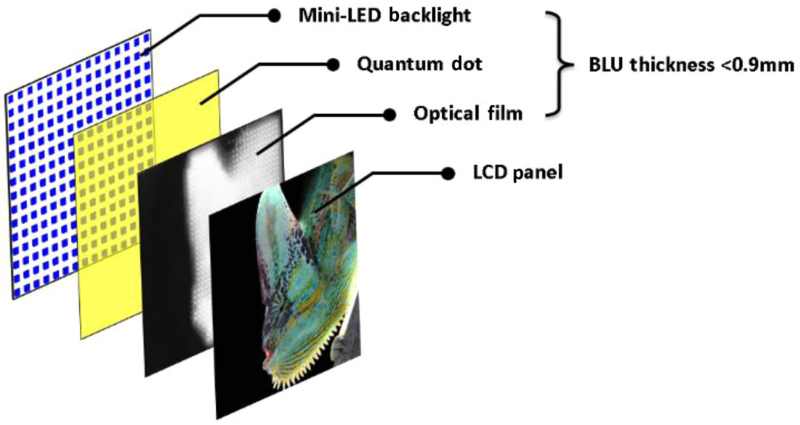

Fig. 12 Backlight module thickness is controlled below 0.9 mm with the zero OD design.

3 Prototype and Specification

The specifications of the ultra-high resolution VR LCD are summarized in Fig. 13. The LCD panel provides a high quality 4K by 4K resolution image with 2117 PPI and ~40 PPD. The slim VR display system incorporating Pancake optics reduces the size of the VR headset while delivering a high-definition, fully immersive experience. Pancake lens optics in VR refer to a compact and lightweight optical design used in VR headsets. These lenses are slim, offer a wide field of view (FOV), minimize distortion, and significantly improve comfort and immersion in the VR experience.

4 Comparing VR Display Technologies

The comparison of various display technologies for VR applications reveals distinct advantages and disadvantages. Micro OLEDs, particularly those based on silicon, hold promise for high-resolution VR experiences, but their cost poses a challenge. Although VR LCD struggles with color contrast and pixel size issues, it excels in offering a wider FOV. The incorporation of mini-LED backlighting substantially improved the LCD's performance, making it competitive with micro OLEDs, especially in terms of response time, contrast, luminance, and lifetime. However, LCD's choice is primarily driven by its ability to achieve larger panel sizes for an immersive experience. Micro OLEDs and micro LEDs, with their smaller sizes, are positioned for high-end markets like Apple's Vision Pro, though they come at a premium cost. On the other hand, a LCD remains a more affordable option, targeting a broader mainstream audience. In summary, each display technology presents a unique set of advantages and limitations, catering to different segments within the VR display industry (Table 2).

2117 ppi VR LCD DEMO	
Size	2.56"
Resolution	3840 x 3840
PPI	2117
Active Area (mm)	46.080 x 46.080
LC Mode	AAS
Color Gamut (NTSC)	97%
Response Time (ms)	< 5 (G2G Max.)

Fig. 13 2.56" VR display specification.

Table 2 Comparing VR display technologies.

Display technology	Pros	Cons
LCD	Wider FOV Affordable option for mainstream users	Color contrast, response time, and color pixel size limitations
Mini-LED backlit LCD	Wider FOV Improved color, contrast, and luminance	Thicker module compares to other display
	Better lifetime than micro-OLED	
Micro-OLED (wafer base)	High potential for high resolution VR	Premium cost for high-end markets like Vision Pro
	Small form factor for high-end applications	Complicated optical design for smaller panel size
Micro-LED (wafer base)	Small form factor for high-end applications	Limited availability of high-resolution VR products

5 Conclusion

In this paper, we addressed several challenges related to high-resolution VR LCD. We discussed how subpixel rendering can help overcome manufacturing limits to achieve 2117 PPI for VR LCDs. Additionally, we improved the LC efficiency of LCDs with small pixels and enhanced their light transmittance. Furthermore, we discussed driving methods to reduce overall power consumption. To achieve HDR and improve contrast and color in high-resolution LCDs, we utilized mini LED backlight technology. We also introduced the concept of higher partitioning to enhance the image quality of high-resolution VR displays. Finally, we proudly announced our industry-first 4K VR LCD with ~40 PPD, which provides good visual detail and immersion in VR. This breakthrough in display technology represents a significant advancement in the development of VR applications, and we are thrilled to see its impact on the industry.

Data availability

Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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