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Special Section Guest Editorial: Advanced Plasma-Etch Technology

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Plasma etch technology is an integral and indispensible part of patterning technology that has enabled continuous scaling in the semiconductor industry for more than forty years. Advancement in plasma-etch technology, along with other semiconductor process technologies, has brought the state-of-the-art semiconductor technology, the so-called 22 nm node of complementary metal–oxide–semiconductor (CMOS) technology, into mass production. This 22 nm node CMOS technology features a three-dimensional (3-D) FinFET, a metal one pitch of about 90 nm and copper/low-k interconnects. The next generation of 14 nm node CMOS technology is expected to be brought into mass production in the first quarter of 2014.

Advanced plasma etch technology and its integration with advanced lithography technology will play an increasingly important role in nanopatterning beyond 22 nm node of CMOS technology and advanced memory technologies. In particular, innovations in plasma etch technology are required to address challenges of resolution, pattern quality, and pattern uniformity of new lithography technologies for sub-22 nm CMOS technology nodes and 1X nm node of advanced memory technologies, particularly 3-D NAND flash memory technology. The candidate lithography technologies include multiple (double or quadruple) patterning with 193 nm immersion lithography, self-aligned double patterning (SADP) or self-aligned quadruple (SAQP) using spacer-image-transfer (SIT), extreme ultraviolet (EUV) lithography, multiple-e-beam direct-write lithography as well as directed self-assembly (DSA) patterning.

Key patterning challenges in sub-22 nm CMOS technology and advanced memory technologies include resolution, pitch shrinking, 3-D structures, new materials, high aspect-ratio etching, overlay control and pattern quality, such as critical dimension uniformity (CDU) and line-edge roughness (LER).

This JM3 Special Section on Advanced Plasma-Etch Technology contains ten overview and original papers. They address the challenges of plasma-etch technology for nanopatterning at 22 nm node of CMOS technology and beyond.

The paper by Wise provides an overview on plasma-etch technology for nanopatterning at 14 nm and 10 nm nodes of CMOS technologies, including multiple patterning techniques such as litho-etch-litho-etch, sidewall image transfer, line/cut mask and self-aligned structures. This paper also discusses advanced plasma-etch processes such as trilayer etches, aggressive CD shrink techniques, and the extension of resist trim processes.

The papers by Xu et al. and Hody et al. address plasma-etch technology for double patterning with 193 nm immersion lithography and extreme ultraviolet (EUV) lithography. These two papers discuss some of the key issues in double patterning, including line-edge roughness (LER) and critical dimension uniformity (CDU). The Xu et al. paper demonstrates 15 nm half-pitch dense line patterns.

Directed self-assembly (DSA) patterning with block copolymers offers a tantalizing possibility of sub-lithography patterns without the need for more costly projection optical lithography tools. DSA patterning relies on the self-assembly of block copolymers (BCPs) directed by lithographically defined template patterns to produce sub-lithography grating-like structures. The paper by Tsai et al. presents an optimization of DSA etch transfer processes with a trilayer film stack for circuit relevant patterning in sub-30 nm pitch regime. The paper by Satake et al. discusses the effect of oxygen addition to an argon plasma on the etching selectivity of poly(styrene)-block-poly(methyl methacrylate) (PS-PMMA) block copolymer. A mixed argon-oxygen plasma was used to fabricate a PS mask pattern with a full-pitch in the range of 25.5 to 77 nm. This work opens up the possibility of an all-dry plasma-etch process to generate the block copolymer etch mask for DSA patterning.

Three papers in this special section cover line-edge roughness. The paper by Azarnouche et al. investigates the impact of various plasma treatments on the line-edge roughness of dense and isolated photoresist patterns prior to patterning transfer and its transfer during gate patterning. The paper by Constantoudis et al. presents a three-dimensional geometrical modeling of plasma transfer effects on line edge roughness. Finally, the paper by Fouchier and Pargon presents an atomic force microscopy metrology technique to study photoresist sidewall smoothing and line edge roughness transfer during gate patterning.

The paper by Tao et al. demonstrates a wet etching technique to form a template of pyramidal silicon nanopore arrays. The authors use the template of pyramidal silicon nanopore array to fabricate sub-100 nm metallic nanocube arrays.

Last, the paper by Winroth et al. explores three 193 nm implant photoresist curing methods, including laser-, ion-, and electron-based treatments to enhance shrink and patterning controls.

We hope that this JM3 Special Section on Advanced Plasma-Etch Technology will prove valuable to the engineers and the researchers in the fast-moving semiconductor industry. We also hope that it will help readers understand the state-of-the-art of semiconductor technology. We further hope that it will serve as a useful reference for those who are interested in nanofabrication, micro- and nanofluidics, micro- and nanophotonics, organic electronics, biochips, photovoltaic (PV), light emitting diode (LED), and other micro- and nanofabrication technologies.

We are grateful for the opportunity to assemble this JM3 Special Section on Advanced Plasma-Etch Technology. We thank all the authors for contributing their latest work to this JM3 special section. We also thank the reviewers for spending the time to carefully review the manuscript and for offering thoughtful comments and suggestions to improve the quality of the manuscripts. Finally, we extend our sincere thanks to the JM3 staff for their tireless efforts and their meticulous organizational skills to help assemble and publish this JM3 special section.

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