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Abstract. An in-line inspection method for estimating defect resistances from the grayscale of voltage contrast in scanning electron microscope (SEM) images of manufactured patterns was developed. This method applies a circuit simulator to calculate the intensity of the secondary electrons according to an equivalent-circuit model considering the charge-up voltage on the patterns. To accurately estimate the resistance of defects formed in a device, first, the simulator was improved by considering the variation in defect resistance, which strongly depends on the differential voltage between the plug surfaces and the backside wafer. The defect resistances were obtained from the measured current-voltage (I-V) characteristics of the intentional defect on the standard calibration wafers, in which some incomplete-contact defects were systematically formed. Next, to consider the effect of the electronic characteristics of the pattern under the normal plugs on the grayscale, the I-V characteristics of the normal plugs were measured. The equivalent circuit of the simulator was improved by taking into account the measured I-V characteristics. The calibration curve for the manufactured patterns was calculated from the improved circuit simulator. Finally, the inspection method was applied to estimate the resistance of defects formed on an static random access memory (SRAM) pattern. The calculated calibration curve was used to estimate the defect resistance from the voltage contrast formed on the defects in the manufactured SRAM patterns. The accuracy of the estimation was about an order of magnitude. [DOI: 10.1117/1.JMM.11.2.023008]

Subject terms: inspection; grayscale; defect; voltage contrast; scanning electron microscopes; I-V characteristics; static random access memory.

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1 Introduction

The scaling down of integrated devices has increasingly necessitated the development of metrology and inspection methods using electron beams. For example, an inspection method using scanning electron microscope (SEM) images has the capability to detect small defects that may be optically invisible at present. The critical defect size in 32-nm half-pitch devices is now 14 nm.[1] In addition, SEM inspection using voltage contrast images, which is affected by the charge-up voltage due to the electron scanning, has the capability to detect electrical defects (such as incomplete-contact defects and shorts). In particular, the authors have already reported that the grayscale of such SEM images depends on the variation in defect resistance due to an incomplete contact.[2–5]

The prospective process flow applying our developed in-line resistance inspection using a noncontact type SEM inspection system is shown in Fig. 1. If the defect resistance of the contact holes can be estimated from the voltage contrast of SEM images of defects, the state of the device production process, namely, process parameters such as etching time, could be fed back to the production stages earlier without the need for performing destructive analysis. In the first stage of the process flow (the gray feedback line in Fig. 1), incomplete-contact defects are classified according to the grayscale level of their voltage contrast. Detected defects are then selectively sampled and destructively analyzed by SEM or transmission electron microscope (TEM). In the second stage (the black feedback line in Fig. 1), defect resistance is estimated from the voltage contrast of the SEM images. According to the estimated defect resistance, the process parameters are fed back and destructive analysis is unnecessary. Up until now, however, defect resistances (which appear as a difference in grayscale) have not been quantitatively estimated during conventional in-line inspection.

The authors have recently developed an in-line inspection method for roughly measuring defect resistance, which is quantitatively estimated from the voltage contrast formed in an SEM image of an incomplete-contact defect. In a previous study, we calibrated the resistances of an incomplete-contact defect from grayscales of defect patterns intentional on the test elementary groups.[6] Except for test elementary groups, however, manufactured patterns in various devices are difficult to inspect because the grayscales of normal-contact plugs and defective plugs formed for manufactured devices may vary according to the resistances between the normal contact plugs and the backside wafer. In other words,

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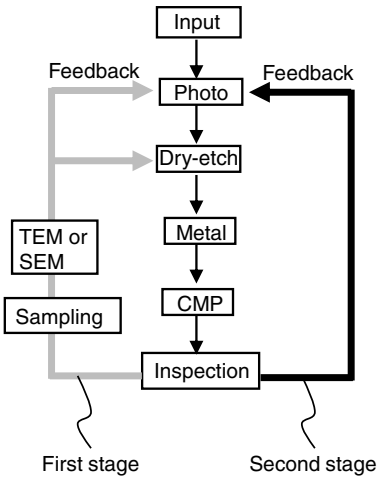

Fig. 1 Prospective process flow applying in-line resistance inspection.

the grayscales of the defective plugs depend on the electrical characteristics of the circuits connected under the plug pattern.

In the present study, we developed a method for estimating defect resistances from the grayscale of voltage contrast formed on manufactured patterns in various devices. This method applies a circuit simulator (which has already been reported[7]) that calculates the charge-up voltage on the patterns and the intensity of the secondary electrons according to an equivalent circuit model. To accurately estimate the resistance of defects formed in a device, the circuit simulator was improved by taking the variation in defect resistance into account, which strongly depends on the differential voltage between the plug surfaces and the backside wafer. At first, the I-V characteristics of the intentional defects on the standard calibration wafers, in which intentional defects were systematically formed, were measured and used to determine the defect resistance of the equivalent circuit. The resistances of the intentional defects were controlled by the thickness of the thin SiO_2 film at the bottom of the contact plug. Next, the measured I-V characteristics were used to determine the resistance of the equivalent circuit of a normal-contact plug formed in the manufactured patterns. Finally, the inspection method was applied to estimate the resistance of defects formed on an static random access memory (SRAM) pattern.

2 Method for Estimating Defect Resistance by Circuit Simulation

We have already reported a circuit simulator that calculates the intensity of the secondary electrons according to an equivalent-circuit model,[7] which considers the charge-up voltage of the plug pattern. Figure 2(a) shows a schematic illustration of the electrical current flow during the electron irradiation to the pattern surface. When the electron beam is irradiated onto a plug pattern, secondary electrons and backscattered electrons are emitted from the plug surface. In case the probe current of the incident electron beam is smaller than the total intensity of the emitted electrons, namely, the total intensity of the secondary and backscattered electrons, the plug surface is positively charged. The positive charge on the plug surface creates a potential barrier (V_B), which is caused by the difference between the charge-up voltage on the plug surface and that on the surrounding SiO_2 formed on the plug pattern.[3] The secondary electrons that have less kinetic energy than the V_B return to the plug surface. The value of V_B, which is maximum potential on the normal line of the top surface of the plug, is determined from the calculation of the electric field distribution from the external electric field on the wafer surface, the charging voltage on the plug surface (V_p) and that on the surrounding SiO_2 (V_0), and the diameter of the plug. In this model, the effective yield of the secondary electrons ($L \cdot \sigma_{SE}$) is determined from the yields of the secondary electrons emitted from the plug surface when the plug surface is not charged (σ_{SE}), and the transmittance of the secondary electrons to the detector (L). The value of L is determined by the proportion of the secondary electrons, which have more kinetic energy than the V_B, emitted from the plug surface. That is, the value of L is determined by the integral of

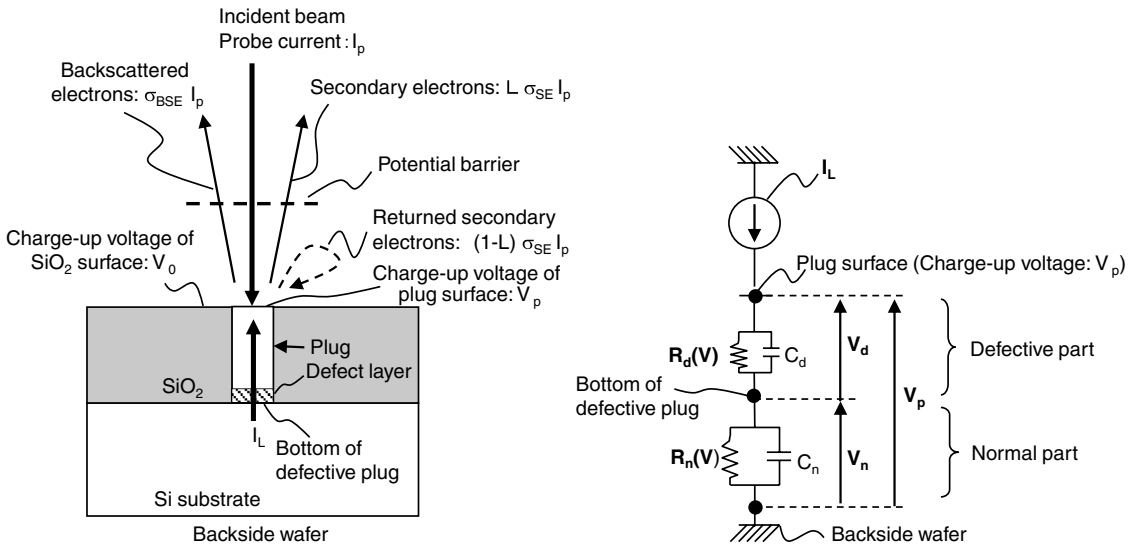

Fig. 2 Schematic illustration of the equivalent-circuit model.

the energy distribution of the secondary electrons when the electron energy is higher than V_B. The electrical current, which flows out a plug, namely, I_L, is given by the following equation:

$$I_p + I_L = L \cdot \sigma_{\mathrm{SE}} \cdot I_p + \sigma_{\mathrm{BSE}} \cdot I_p,$$

where I_p is the probe current of the incident beam, and σ_{BSE} is the yields of the backscattered electrons emitted from the plug surface when the plug surface is not charged. The total effective current due to the secondary electrons ($L \cdot \sigma_{\mathrm{SE}} \cdot I_p$) and the backscattered electrons ($\sigma_{\mathrm{BSE}} \cdot I_p$) are relatively measured from the gray scale of the voltage contrast formed on the SEM images. In this simulation, I_p is assumed to be steady current and the current flew till V_p becomes steady state.

The current that flows through the defective plugs is determined by the equivalent-circuit model shown in Fig. 2(b). The equivalent circuit of the manufactured pattern is divided into the defective part and the normal part composed of the pattern under the plug. The defective part is the equivalent—circuit between the plug surface and the bottom of the defective plug, and the normal part is that between the bottom of the defective plug and the backside wafer. To accurately estimate the resistance of defects formed in a device, the defective part of the equivalent circuit was improved by taking the variation in defect resistance into account. The measured I-V characteristics of the intentional defects on the standard calibration wafers provide the defect resistance $[R_d(V)]$ of the equivalent circuit. The resistance of the circuit under the normal plug $[R_n(V)]$ is measured from the I-V characteristic between the normal plug surface and the backside wafer. The differential voltage between the plug surface and the backside wafer (V_p) is divided into two: defective-plug voltage (V_d) and pattern-under-the-plug voltage (V_n). In the circuit simulator, the electrical current (I_L) that flows through the defective plug is determined from V_d and the I-V characteristics of the intentional defect. Figure 3 shows our developed inspection process flow for estimating defect resistances formed on manufactured patterns in various devices. Before the in-line inspection process, the parameters of the circuit simulator are calibrated by measuring voltage contrast formed on a standard calibration wafer. The resistance of the normal plug on the manufactured wafer is then measured by a nano-prober, and the calibration curve for the manufactured wafer is calculated from the improved circuit simulator. After this off-line calculation process, the defect resistance is estimated from the voltage contrast formed on the manufactured wafer.

3 Standard Wafer for Voltage-Contrast Calibration

3.1 *Wafer Preparation*

Standard calibration wafers, which have been already reported,[6] for measuring the I-V characteristics of the incomplete-contact defects were prepared. A schematic cross section of a standard calibration wafer is shown in Fig. 4. Contact plugs with a diameter of 0.16 μm were fabricated on a 300 mm diameter p-type silicon wafer. Defective plugs, in which the contact resistances were precisely controlled, were systematically formed. A thin SiO_2 film was formed at the bottom of a defective plug, i.e., an incomplete-contact defect. The resistance of the defects was controlled by the thickness of the thin SiO_2 film at the bottom of the contact plug. Three types of wafers, in which the SiO_2 thickness of the defects on each wafer was uniformly controlled, were prepared. To precisely control the thickness of the SiO_2 film at the bottoms of the contact plugs, these wafers were prepared by the following process. First, normal hole patterns were fabricated on the wafer. A thin SiO_2 film, in which the thickness was then precisely controlled, was formed on the normal contact-hole patterns. These wafers were prepared with high-, medium-, and low-resistance defects. Afterwards, the thin SiO_2 films on the normal hole-patterns were removed by using a mask fabricated for these standard calibration wafers. The holes were then filled in to complete the contact-plug patterns with systematically formed defects.

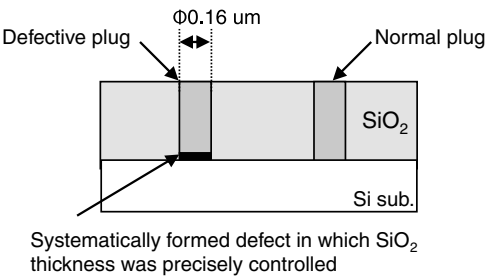

Fig. 4 Schematic cross section of a standard calibration wafer.

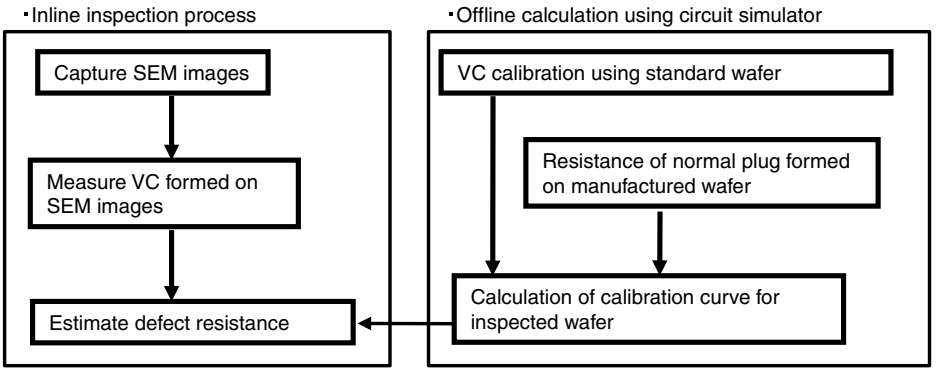

Fig. 3 Inspection process flow for estimating defect resistances formed on manufactured patterns in various devices.

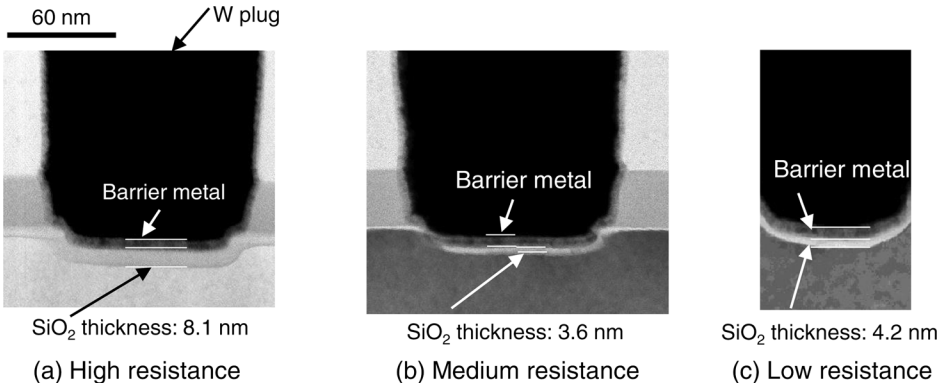

Fig. 5 Cross-sectional TEM images at the bottoms of the defective plugs with three varieties of resistances.

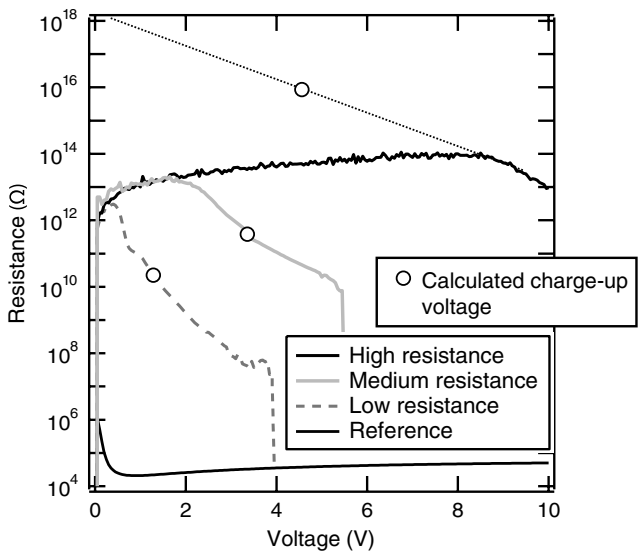

Fig. 6 Resistance of defects measured with a nano-prober as a function of differential voltage between W plug and Si substrate.

3.2 *Analytical Results*

We analyzed the prepared standard calibration wafers by using cross-sectional TEM and measured their I-V characteristics. Cross-sectional TEM images of the bottoms of the defective plugs are shown in Fig. 5. Uniform SiO_2 films were observed at the bottom of the high- and medium-resistance defective plugs. The measured thickness of the SiO_2 film at the bottom of the high-resistance defective plug is 8.1 nm, and that of the medium-resistance defective plug is 3.6 nm. The measured thickness of the film at the bottom of a low-resistance defective plug is 4.2 nm, but the bottom shape is different from those of the other images and the film is not as uniform as that in the other images. Accordingly, the film at the bottom of the low-resistance defective plug is thicker than that of the medium-resistance one.

The I-V characteristics of these intentional defects were measured with a nano-prober.[8] A probe contacting the W-plug surface was biased, and its current was measured. The silicon substrate was connected to the ground. The I-V characteristics between the surface of the W-plug and the silicon substrate were then measured. The resistance of the intentional defects as a function of the differential voltage between the W-plug and the silicon substrate is plotted in Fig. 6. This figure shows that the defect resistance strongly depends on the differential voltage between the plug surfaces and the backside wafer. Accordingly, the defect resistance strongly depends on the charge-up voltage during electron irradiation. The resistance of the high-resistance defect with an 8.1-nm-thick SiO_2 film slightly increased, i.e., from 10^{12} to 10^{14} Ω when the voltage increased from 0 to 8 V because the actual resistance was higher than the measurement limit of the nano-prober in this voltage range. However, the resistance decreased from 10^{14} to 10^{13} Ω when the voltage increased from 8 to 10 V. Accordingly, the resistance when the voltage ranged from 0 to 8 V was roughly estimated from that when the voltages ranged from 8 to 10 V. The resistance of the medium-resistance

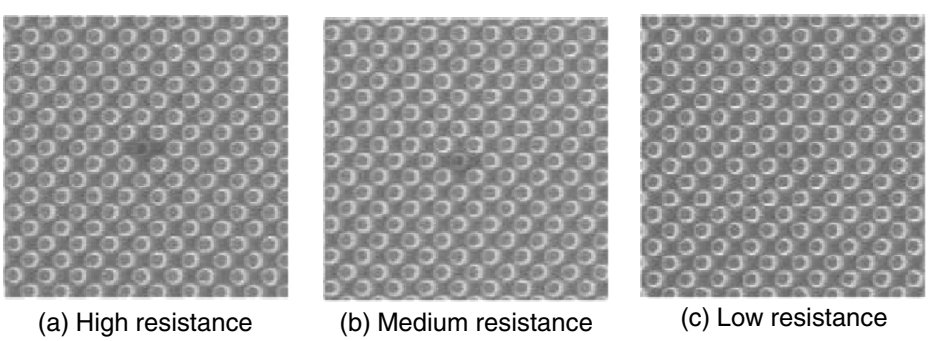

Fig. 7 SEM images of an intentional defect on standard calibration wafers.

defect with a 3.6-nm-thick SiO_2 film decreased from 10^{13} to 10^{10} Ω when the voltage increased from 2 to 5 V. The resistance of the low-resistance plug decreased from 10^{13} to 10^{8} Ω when the voltage increased from 0 to 4 V. The resistance of the defective plug can therefore be precisely controlled by the SiO_2 film formed at the bottom of the plug. The measured I-V characteristics of the intentional defects formed on these wafers are suitable as typical electrical characteristics of the defective part of the equivalent circuit.

SEM images of the intentional defects are shown in Fig. 7. The landing energy of the electron beam was 0.8 keV, and the probe current was 60 pA. The high-resistance defect is easily detected because the image of the defective plug is remarkably dark. The images of the medium- and low-resistance defects are less clear than that of the high-resistance defect. This result shows that the gray scale of a defect plug depends on the resistance of the defect.

3.3 *Simulation Results for Standard Calibration Wafer*

The gray scales of the SEM images shown in Fig. 7 were compared with the calculated gray scales from the equivalent-circuit model. Figure 8 shows a calibration curve calculated from the equivalent-circuit model considering the measured I-V characteristics of the defects. Probe current I_p was 60 pA. When the landing energy of the electron beam was 0.8 keV, σ_{SE} was supposed to be 1.05 and σ_{BSE} was supposed to be 0.4; when the landing energy of the electron beam was 1.0 keV, σ_{SE} was supposed to be 0.9 and σ_{BSE} was supposed to be 0.45. These values of the yields are consistent previously reported ones.[9–11] The voltage contrast was determined from the difference between the total intensity from the normal plugs and that from the defective plug. It was normalized by the difference between the total intensity from the normal plugs and that from the surrounding SiO_2 area. The calculated voltage contrasts completely agree with those formed in the SEM images shown in Fig. 7. The differences between the calculated and measured results are less than 1.0% because the charge-up voltage on the defective plug is accurately calculated in consideration of the variation

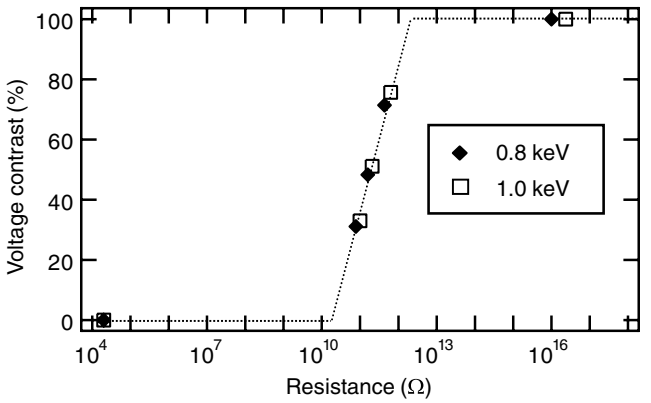

Fig. 8 Calibration curve obtained from the calculation considering measured I-V characteristics of defects formed on standard calibration wafers.

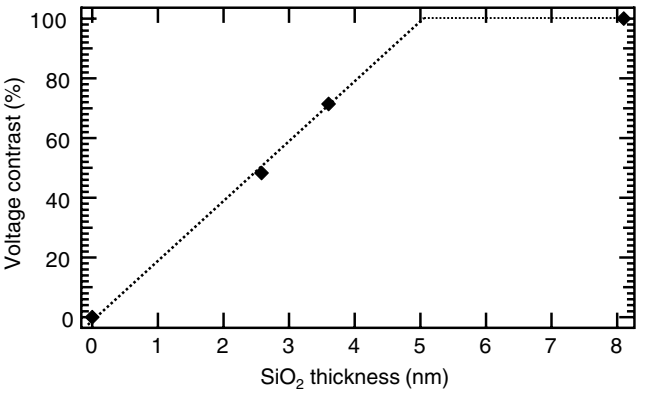

Fig. 9 Calibration curve for SiO_2 thickness at bottom of defect.

in the defect resistance, which widely varied with varying differential voltage between the defective plug surface and the backside wafer, as shown in Fig. 6. However, it is difficult to measure the charge-up voltage on each defective plug during electron irradiation. The open circles plotted in Fig. 6 represent the defect resistances at the charge-up voltage calculated by the circuit simulator considering the variation in the defect resistances of the defective plugs. This result shows that the charge-up voltage of the defective plug depends on the defect resistances. However, the difference between the simulated resistance and the measured resistance possibly becomes larger than 1.0% using a different SEM system. This difference mainly caused by the assumption of the energy distribution of the secondary electrons. This difference should be minimized by adjusting a parameter of the function L, which is determined from integrating the energy distribution of the secondary electrons when the electron energy is higher than V_B.

Figure 9 shows a calibration curve for SiO_2 thickness at the bottom of the defect. It is noteworthy that the SiO_2 thickness calibrated by these standard wafers is not exactly the same as the SiO_2 thickness of the defective plug formed in the manufactured wafer, because the electrical conductivity of the residual SiO_2 films at the bottom of the plugs slightly vary. However, the thickness of SiO_2 is roughly estimated from the grayscale formed on the SEM image.

4 Estimation of Resistances of Defects Formed on SRAM Patterns

4.1 *Experiments*

Plug patterns on a wafer manufactured for an SRAM device were inspected using the developed in-line inspection method. At first, dark defects were detected by using an EB inspection system, i.e., a Hitachi High-Technologies I-5320. Next, the detected dark defects were reviewed by defect-review SEM, which, as explained above, was used to improve the equivalent-circuit model of the defective part.

To obtain the calibration curve for the SRAM pattern, the I-V characteristics of the normal plugs of the SRAM pattern were measured by a nano-prober. The measured resistances obtained from the I-V characteristics of the normal plugs were used to determine the resistance of the part of the equivalent circuit connected under the plug, shown in Fig. 2(b). As explained above, the resistance of the defective plugs on the standard calibration wafers was input to

simulate the defective part of the equivalent circuit. After the calibration curve for the SRAM pattern was calculated from the improved equivalent circuit model, the resistances of the detected defects were estimated from the grayscale of the voltage contrast formed on the images of the SRAM pattern. Finally, the estimated defect resistances were compared with those measured by the nano-prober.

4.2 *Results and Discussion*

The calibration curve obtained by considering the resistance of the intentional defects and that of the normal plug in the SRAM pattern is shown in Fig. 10. The normal plugs formed on the SRAM pattern are classified into four types. The first type was formed on a p-type diffusion layer; the second type was formed on an n-type one; the third type was connected to a gate electrode; and the fourth type was a shared contact plug connected to both a p-type diffusion layer and a gate electrode. The calibration curve of a plug connected to a p-type diffusion layer is almost the same as that of a shared contact plug. The measured voltage contrasts formed in the SEM images of the four types of normal plug patterns are plotted at the resistance of 10^8 Ω in Fig. 10. The differences between the voltage-contrast calculations and measurements of the normal plugs are less than 8.0%. This calibration curve is applied below for estimating the resistances of defects formed on plug patterns in an SRAM device.

Examples of SEM images of dark defects on a SRAM pattern are shown in Fig. 11. Two types of dark defects are observed on the images of the shared contact plugs. One is a dark defect with higher contrast, as shown in Fig. 11(a), and the other is a defect with lower contrast, as shown in Fig. 11(b).

Variation in voltage contrast formed on a defective plug for shared contacts is shown in Fig. 12. The grayscales are an average of the grayscales of pixels in the area of the defective plug. An error of the grayscales depends on the variation in I_p. To correct this error, the voltage contrast was determined from the difference between the averaged grayscale of normal plugs and that of a defective plug. It was normalized by the difference between the averaged grayscale of normal plugs and that of the SiO_2 area in each SEM image. As a result, the voltage contrasts of the defective plugs formed in shared contact patterns are classified as two levels, as shown in Fig. 12. The higher contrasts, which were calculated from the grayscales of the darker defects, are about 100%; the lower contrasts, which were calculated from the grayscales of the slightly dark defects, are from 38% to 60%. The resistances of the dark defects were estimated to be 10^{12} Ω or higher. The resistances of the other defect with lower contrast were estimated to be from 1.0×10^{11} to 3.0×10^{11} Ω. Examples of the resistances measured with a nano-prober at the charge-up voltage are plotted in Fig. 10. The plotted measured resistances were those at the charge-up voltage, which was calculated by the circuit simulator considering the measured IV characteristics of the defect formed on SRAM pattern. The resistance of the darker defect was too high to measure by a nano-prober. The measured resistances of the slightly darker defects agree well with the calculated calibration curve within an accuracy of an order of magnitude. The measured resistance has an error caused by variation in the voltage contrast formed in a field of view image. This variation is mainly due to the beam scan. The standard deviation of the voltage contrast of the normal plug in a field of view image is 12.0%. If the standard deviation of the voltage contrast of the defective plug is equal to that of the normal plug, the accuracy of this method is within an order of magnitude. This method is expected to be more accurate to more precise inspection. However, this accuracy is good enough to classify the defects according to the resistance value. Defects for the destructive analysis are efficiently selected using this method.

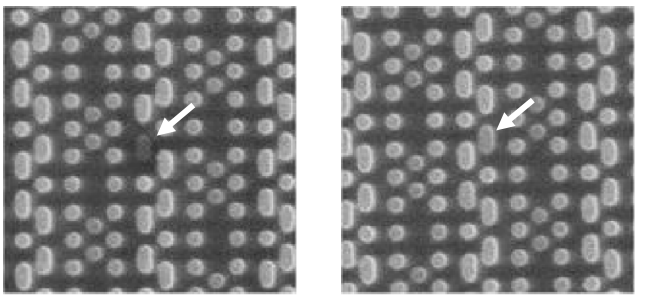

Fig. 11 Examples of SEM images of a defect with higher contrast and a defect with lower contrast on an SRAM wafer.

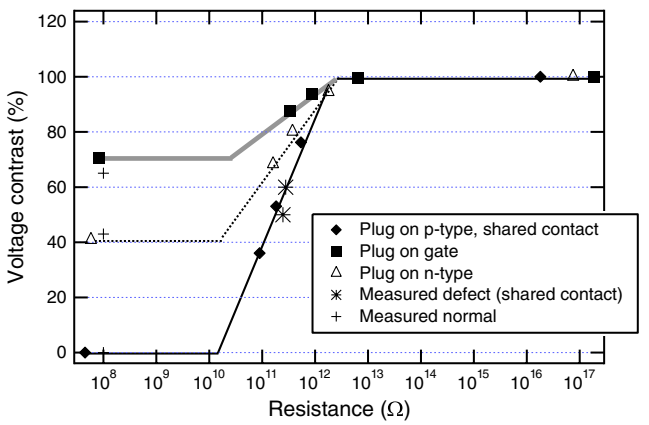

Fig. 10 Calibration curve for SRAM pattern.

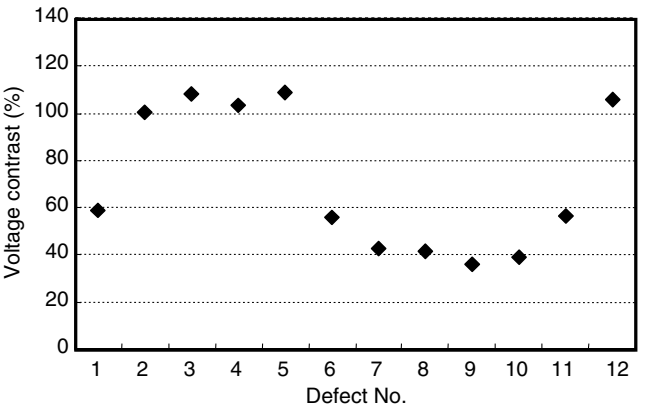

Fig. 12 Variation in voltage contrast measured from defect images formed on a plug for shared contacts. Voltage contrast is separated into two levels.

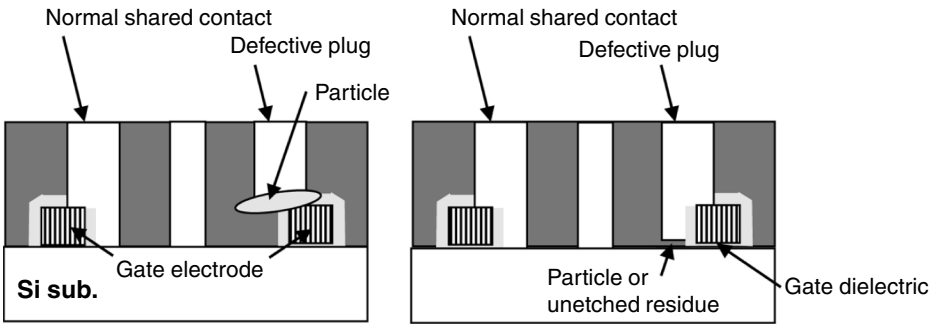

Fig. 13 Schematic cross-sections of a detected defect with higher contrast and a defect with lower contrast.

Schematic cross-sections of defects analyzed by TEM are shown in Fig. 13. A normal shared contact is connected to both a gate electrode and the silicon substrate. However, the defective plugs with higher contrast, shown in Fig. 13(a), are neither connected to the gate electrode nor the silicon substrate. The defective plugs are completely disconnected because of particles such as dust or other residue. The defective plugs with lower contrast, shown in Fig. 13(b), are connected only to the gate electrode, that is, not to the silicon substrate. They are prevented from connecting to the silicon substrate by particles or un-etched residues. Accordingly, positive charges on the plugs might leak through the gate dielectric to the silicon substrate.

5 Summary

An in-line inspection method for estimating defect resistances from the grayscale of voltage contrast in SEM images was developed. Taking charge-up voltage on the manufactured patterns into account, this method applies a circuit simulator that calculates the intensity of the secondary electrons. First, this simulator was improved by considering the variation in defect resistance, which strongly depends on the differential voltage between the plug surfaces and the backside wafer. The defect resistances used in the equivalent circuit of the simulator were obtained by measuring the I-V characteristics of the defect formed on standard calibration wafers. As a result, the calculated voltage contrasts completely agree with the measured voltage contrasts. Next, the calibration curve for the SRAM pattern was calculated using this simulator. The equivalent circuits connected under the plug were obtained from measuring the I-V characteristics of the normal plugs on the SRAM pattern. Finally, this in-line inspection method was applied to estimate the resistance of defects formed on an SRAM pattern. The grayscales of detected defects formed at the bottom of shared contact patterns were classified as two levels. The higher contrasts, which were calculated from the grayscales of the darker defects, were about 100%; the lower contrasts, which were calculated from the grayscales of the other defects, were from 38% to 60%. The defect resistances were estimated from the obtained calibration curve. The estimated resistances of the defects with higher contrast were 10^{12} Ω or higher, and those of the other defects with lower contrast were from 1.0×10^{11} to 3.0×10^{11} Ω. The estimated resistances of the defects (with an accuracy of about an order of magnitude) agree well with the resistances measured by a nano-prober.

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