Journal of Astronomical Telescopes, Instruments, and Systems

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Abstract. We report our progress toward optimizing backside-illuminated silicon P-type intrinsic N-type complementary metal oxide semiconductor devices developed by Teledyne Imaging Sensors (TIS) for far-ultraviolet (UV) planetary science applications. This project was motivated by initial measurements at Southwest Research Institute of the far-UV responsivity of backside-illuminated silicon PIN photodiode test structures, which revealed a promising QE in the 100 to 200 nm range. Our effort to advance the capabilities of thinned silicon wafers capitalizes on recent innovations in molecular beam epitaxy (MBE) doping processes. Key achievements to date include the following: (1) representative silicon test wafers were fabricated by TIS, and set up for MBE processing at MIT Lincoln Laboratory; (2) preliminary far-UV detector QE simulation runs were completed to aid MBE layer design; (3) detector fabrication was completed through the pre-MBE step; and (4) initial testing of the MBE doping process was performed on monitoring wafers, with detailed quality assessments. [DOI: 10.1117/1.JATIS.1.4.046001]

Keywords: ultraviolet astronomy; complementary metal oxide semiconductor; backside Illumination; HyViSI™; focal plane array; molecular beam epitaxy; silicon P-type intrinsic N-type.

Paper 15004P received Jan. 15, 2015; accepted for publication Aug. 11, 2015; published online Sep. 11, 2015.

1 Introduction

Recent advances in the ultraviolet (UV) responsivity of silicon-based focal plane imaging arrays enable new lighter-weight, lower-power, and less-complex UV instrument concepts for the investigation of planetary atmospheres. An initial one-year program was conducted to optimize backside-illuminated silicon P-type intrinsic N-type (PIN) complementary metal oxide semiconductor (CMOS) devices developed by Teledyne Imaging Systems (TIS) for far-UV planetary science applications. This UV-optimized CMOS detector, built in collaboration with TIS and MIT Lincoln Laboratory (LL), will enable more compact, low-power, low-mass, and larger-format UV focal plane array systems suitable for Discovery missions to the outer planets and their satellites, Mercury, Venus, Mars, and comets.

1.1 *Need for Advanced Far-UV Spectrographs on Planetary Missions*

The exploration of planetary atmospheres using UV spectroscopy has played an important role in NASA's exploration of the solar system on the vast majority of Flagship-class and New Frontiers missions to date. This includes a long line of notable discoveries by the Pioneers, Mariners, and Voyagers across the solar system. More recently, this includes the Galileo/Ultraviolet Spectrograph (UVS) at Venus and Jupiter; the Cassini/Ultraviolet Imaging Spectrograph at Venus, Jupiter, and Saturn; Rosetta Alice at Mars, asteroids Steins and Lutetia, and comet 67P/Churyumov-Gerasimenko (August 2014); New Horizons Alice at Jupiter and Pluto (July 2015); and high expectations for the Juno UVS, now en route to Jupiter, and for the Jupiter Icy Moons Explorer UVS in development. In surprising contrast, only 2 of the 15 Discovery and Mars Scout class missions selected by NASA to date include UV spectrographs (MESSENGER/MASCS and MAVEN/IUVS).

In many ways, the initial survey of the solar system with UV spectrographs is complete. Future missions including UV measurements will have increasingly focused objectives and related design requirements for low-resource instruments in the same stratagem as the Discovery line of missions. The current lack of UV instrument designs requiring very low resources, and the lack of diversity in capabilities for those UV instruments currently flying, explains in part the dearth of UV spectrographs on Discovery-class missions. In many cases, two or more detectors and/or different photocathodes are selected for extreme-UV, far-UV, and/or mid-UV coverage in order to maintain high quantum efficiency (QE) (i.e., $>10\%$) across the entire bandpass.[1] The need to better adapt UV measurement techniques for small-class missions motivates us to diverge from the low-light level imaging requirements typical for most far-UV imaging spectrograph designs found today. Instead, our aim is to develop new detector technologies free of gain degradation and optimized for bright UV solar and stellar occultation targets—a

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powerful remote observing method for characterizing planetary atmospheres.

1.2 *Recent Advances in Hybridized CMOS Silicon Imaging Arrays*

CMOS detector technology is advancing at a furious pace and is now widely used for visible- and IR-wavelength applications. These include cell phone cameras on the low end and high-end custom arrays for IR astronomy, such as those built for NASA's James Webb Space Telescope. The potential for UV applications with these devices is at its infancy, and we aim to develop this field with this research project. Continued miniaturization of electronics for these devices provides reductions in mass and power with greatly increased capabilities, and the potential for further advances in this technology is high, while microchannel plate (MCP) and charge-coupled device (CCD) technology is mature.

2 Need for UV Optimization of Hybridized CMOS Devices

2.1 *Initial UV-Optimized Silicon P-Type Intrinsic N-Type Detector Development*

TIS created a new line of wide-area silicon diodes that are sensitive to mid-UV light (>200 nm) in addition to visible wavelengths.[2] While still in the prototype stage, TIS has demonstrated >30% sensitivity to light at 200 nm (Fig. 1), which makes the potential for UV applications very promising in the 110 to 310 nm range. These silicon detectors operate with a bias voltage of +5 to +30 V, orders of magnitude lower than MCP detectors and within the range of existing low-voltage power supplies. Furthermore, these detectors are radiation hard due to both the inherent thinness of the CMOS devices and additional radiation-hardened designs and processes.[2] Last, as advanced commercial detectors develop improved capabilities, the cost for including these new technologies for higher performance in specialty devices like ours is expected to be lowered.

2.2 *Far-UV Performance of Previously Studied Teledyne Imaging Sensors Devices*

Prior to the presently reported study, the sensors described in Ref. 2 were tested by Southwest Research Institute (SwRI) to measure their responsivity at far-UV wavelengths (100 to 200 nm).[2,3] These devices were not passivated using the molecular beam epitaxy (MBE) method. Reference 3 reported the far-UV sensitivities of two different test devices provided by TIS (Ref. 2) using the SwRI Ultraviolet Vacuum Radiometric Calibration Facility.[4] The backside-illuminated measurements of the first single-channel device performed better than those of the front side at far-UV wavelengths, as expected from previous visible light tests. The second device had dual channels with both oxide-coated and visible antireflective coatings, the latter being unsuitable for the far-UV. This initial study demonstrated that the single-channel CMOS detectors are sensitive to UV light at levels ranging from 22% at 121.6 nm to 25% at 160 nm, as shown in Fig. 2 for the oxide-coated device. The sensitivity is measured in QE, which has been corrected for quantum yield using two methods: (1) in the far-UV, a value of 1 electron per 3.65 eV, as reported by Ref. 5, and (2) the method reported by Ref. 6, appropriate at longer wavelengths. The oxide-coated channel of the second device demonstrated a low sensitivity of 6% at 121.6 nm, but an increase up to 40% at 160 nm. Our finding of 25 to 40% sensitivity at 160 nm, measured at room temperature, greatly exceeded expectations for the potential suitability of these devices to future UV studies and is very competitive with MCP type quality. Our presently reported development work was motivated by these early successes.

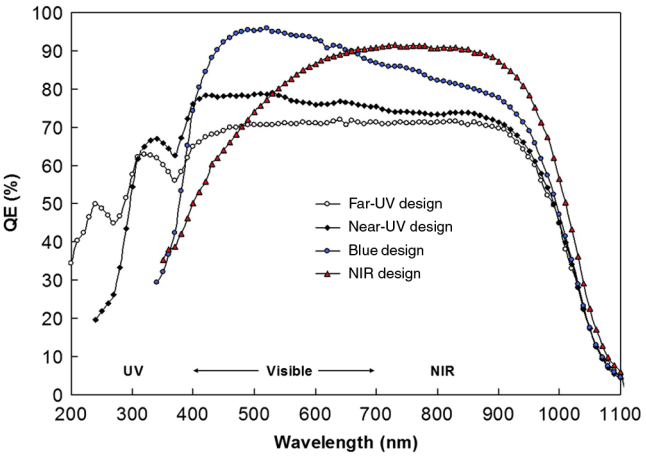

Fig. 1 UV-visible sensitivity of a sampling of silicon PIN sensors as reported with various antireflection (AR) coatings in Ref. 2.

2.3 *Need for Continued Development of UV Optimization for Silicon Imaging Arrays*

Beyond the promising performance of up to 40% sensitivity for far-UV photons, our set of reasons for further developing the TIS UV-optimized large-format backside-illuminated silicon PIN photodiode array with hybridized CMOS readout includes the following examples:

1. The detector does not require a high-voltage power supply, which enables reduced mass (0.5 kg), power (0.5 W), schedule (i.e., lab functional testing in vacuum), and complexity.
2. Low light sensitive MCP devices experience flux-dependent gain degradation (sag) preventing observations of bright, high-fluence targets while fully utilizing the aperture (although we acknowledge that recent developments of atomic layer deposition processes are mitigating this problem, with an in-flight demonstration expected soon).
3. Comparable responsivity (QE) to both far-UV (100 to 200 nm) and mid-UV (200 to 300 nm) should be obtained within this one device; in comparison, two MCPs coated with different photocathode materials are typically required to achieve this bandpass coverage in planetary missions, further reducing resources.
4. Further improvements to the expected detector performance from 100 to 200 nm enhance the sensitivity to more molecular species (methane and other hydrocarbons) and add more stellar occultation targets for planetary atmosphere studies.
5. Electronic control of the detector with the compact, self-contained SIDECAR ASIC technology currently

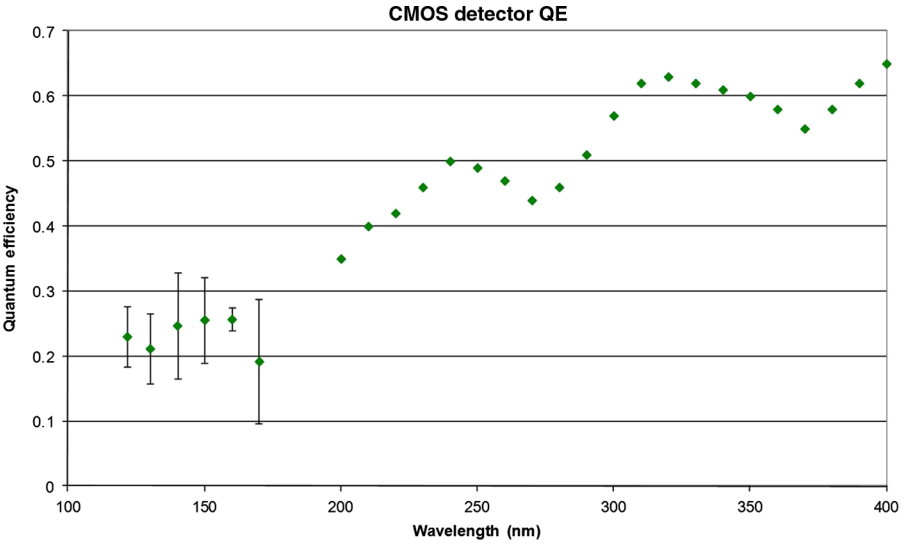

Fig. 2 Backside far-UV measurements performed at Southwest Research Institute,[3] shown with error bars, along with the mid-UV measurements made by Teledyne.[2] Quantum yield effect[5,6] has been taken into account in both data sets such that quantum efficiency (QE) is the percentage of incoming photons detected. Dips in the sensitivity (QE) at 270 and 370 nm are intrinsic to the optical property of silicon (see Fig. 5), which had an oxide thickness of ~25 to 30 nm. This 25 to 30 nm oxide layer essentially acts as an AR coating, resulting in higher QE than the reflection limit of silicon. The excess at 121.6 nm (relative to the theoretical limit for this oxide thickness) and the dip at 170 nm need further investigation and confirmation with further UV-optimized designs.

available from TIS for these devices[7,8] allows further miniaturization relative to current MCP-based designs (0.75 kg, 4.5 W), with high capability control of digital outputs (especially on-chip integration of analog-to-digital conversion).

6. Demonstrated radiation hardness of ~100 krad for TIS's CMOS devices is an advantage over heavily shielded MCPs and potential CCD-based UV-optimized detectors in the Jupiter system.

7. In certain applications where simultaneous observations of both bright and dim targets is desired (a common occurrence in planetary missions, e.g., when observing both dayside and nightside), the local and global count rate limits common for MCPs are prohibitive in a way that does not apply to the defined dynamic range of CMOS arrays.

8. CMOS arrays are already available with about four times smaller pixel sizes than MCPs (allowing more compact instrument designs), and the trend for CMOS miniaturization is continuing at the same time pixel-based read-out circuit functionality is increasing.

The initial optimization method[2] focused on wavelengths in the 200 to 300 nm mid-UV range. We are pursuing two primary advancements to further improve performance specifically in the 100 to 200 nm far-UV range: (1) use thinner wafers to improve the point spread function in light of the shorter absorption depth of far-UV photons into an Si wafer and to enhance photo-charge collection at a moderate bias, and (2) passivate the backside surface of the silicon PIN detector wafer with an MBE process by setting up a thin surface potential to improve the collection of UV photon generated holes at the illuminated surface. Our approach to the UV optimization of CMOS devices leverages the benefits demonstrated by comparable work for p-channel CCDs, including seminal work on the use of antimony (Sb) doping.[9–14]

3 Doping Thinned Silicon P-Type Intrinsic N-Type Wafers with Antimony

Lincoln Laboratory's Advanced Imager Technology Group collaborated to implement their MBE process[15] to further enhance UV-optimized prototypes developed by TIS and tested at far-UV wavelengths by SwRI. The first step was to identify the thickness of wafers that would still tolerate the stresses involved in both the initial MBE process and subsequent manufacturing steps, such as flip-chip hybridization mating detectors to a read-out integrated circuit. A thickness as small as 100 μm was determined to be readily feasible, with alternative processes prior to MBE likely to enable even smaller thicknesses. An intermediate set of 200 μm wafers and the same 300 μm wafer thickness were used in our work to mitigate the risk of mechanical failure during testing. An initial set of float-zone silicon wafer materials with the three wafer thicknesses (300, 200, and 100 μm) was tested in the MBE growth chamber wafer handling system at LL, and none of the samples fractured.

Following this successful handling test, a set of high-quality float-zone wafers were delivered to LL for the optimization study reported here. This study sample of 12 blank wafers is described in Table 1. Note that no device structures for electrical interfaces reside on these wafers at this time. To test whether scratches or contamination during the shipping of wafers from TIS to LL would be a concern, half of the 12 wafers were cleaned of backside oxides at TIS, while the other half were left with the backside oxide on and processed at LL postdelivery. In both cases, the wafers were processed and handled successfully without incident.

In parallel to the MBE process development, TIS proceeded with the design and fabrication of silicon PIN detector wafers.

Table 1 Wafer test sample set specifications. The sample names Teledyne Imaging Sensors sent to MIT Lincoln Laboratory for testing are denoted by wafer number "W#." Samples were either etched for removal of oxide, or not.

W#	Description	Comment/process	W#	Description	Comment/process	W#	Description	Comment/process
7	100 μm with oxide		**9**	200 μm with oxide		**11**	300 μm with oxide	
8	100 μm with oxide		**10**	200 μm with oxide		**12**	300 μm with oxide	
1	100 μm no oxide	Clipped flat	**3**	200 μm no oxide	MBE 1.25e20 cm^{-3}, 10 nm	**6**	300 μm no oxide	MBE 1.25e20 cm^{-3}, 10 nm
2	100 μm no oxide	MBE 1.25e20 cm^{-3}, 10 nm	**4**	200 μm no oxide	MBE 1.25e20 cm^{-3}, 10 nm	**5**	300 μm no oxide	MBE 1.25e20 cm^{-3}, 10 nm

MBE, molecular beam epitaxy.

Two detector configurations were used: 1K × 1K detector array and discrete diode test array. The 1K × 1K detector wafers were used to produce detector pixel arrays that are to be flip-chip hybridized to Teledyne HAWAII-1RG CMOS readout electronics and the discrete test diode wafers were intended for quick far-UV QE verifications during the processing stages. The MBE process was to be applied at the late stage of the final detector fabrication process. TIS conducted an internal manufacture readiness review to finalize fabrication parameters, allocate resources, and plan the detector fabrication as part of this early design stage.

The photoabsorption depth in silicon (Fig. 3) necessitates that the junctions be located within a depth of ~5 nm (where 100 to 200 nm far-UV photons are registered by the detector). Ion-implanted laser annealing and other methods used, for example, in CCD production, affect deeper 75 to 150 nm regions,[17] making the MBE process essential to our UV-optimization approach. The facilities for applying the MBE process to batches of wafers at LL were recently improved to include a Veeco GEN200 cluster tool including reflection high-energy electron diffraction (RHEED) imaging, residual gas analyzer, and electron impact-energy spectroscopy measurements in the growth module, a preparation module, and an x-ray photoelectron spectroscopy analysis chamber. Together with additional scanning ion mass spectrometry (SIMS) and four-point film-resistivity probe analyses tools, the necessary steps to control and assess the quality of the MBE process were provided in great detail.

Sb was identified as the best dopant material for optimizing the performance of silicon PIN photodiode arrays built on an n-type silicon substrate. Its relatively low vapor pressure makes it easier to use compared with other candidates, such as P or As, which would require special accommodation within the growth chamber cells. Unlike boron-doped Si used to optimize p-type devices like backside-illuminated CCDs with the MBE process, the n-type silicon PIN substrate required us to develop a new approach at LL with a new dopant material. Figure 4 shows an early test of Sb deposition within the MBE growth chamber, since this material had not been previously used at LL. The deposition of Sb proceeded as a function of temperature at rates that were in agreement with equilibrium vapor pressure calculated rates.[18] Each MBE run required ~3 h per wafer for the layer-growth process to complete.

QE modeling was performed in the far-UV range to further guide our design and UV-optimization efforts. The absorption

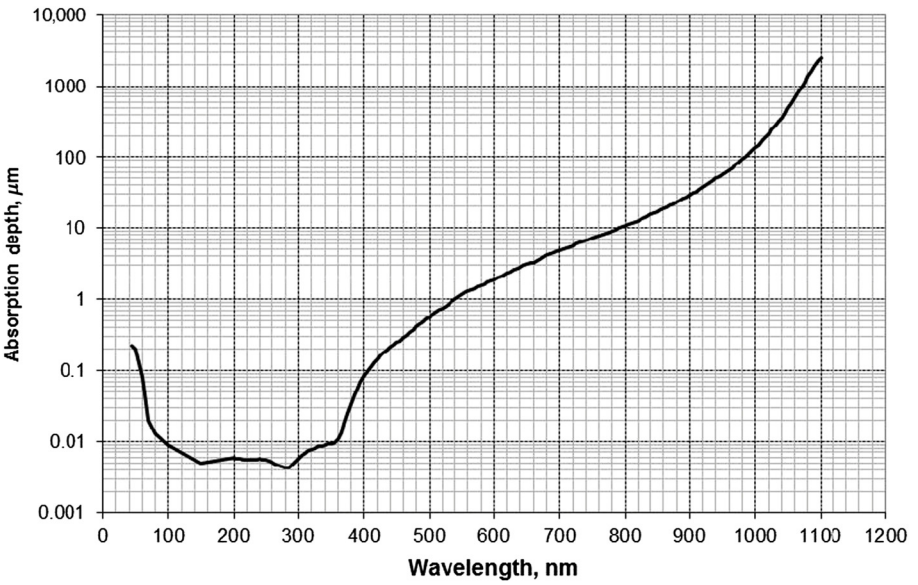

Fig. 3 Photoabsorption depth in silicon.[16]

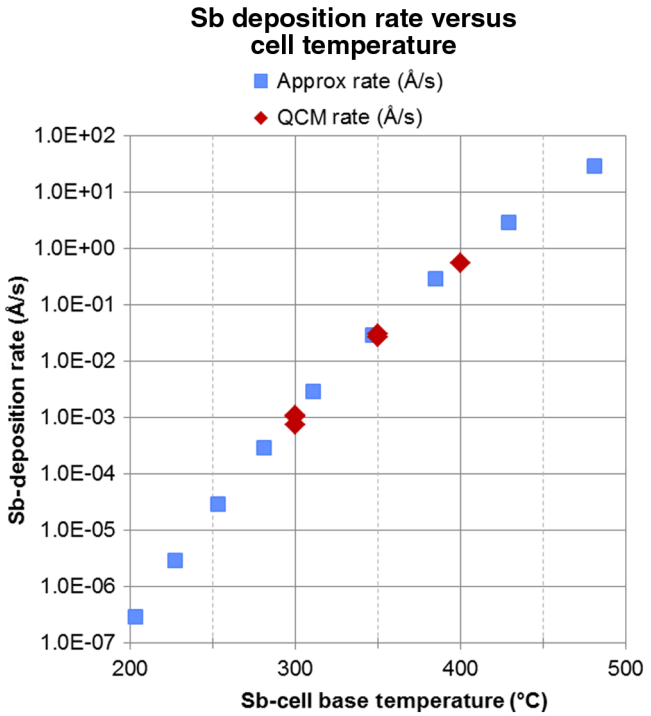

Fig. 4 Molecular beam epitaxy (MBE) deposition of Sb occurred at a rate measured with a quartz-crystal microbalance that was in good agreement with calculated rates based on vapor pressure equilibrium curves,[18] and knowledge of temperature and pressure differences between the standard effusion cell source and the substrate within the growth chamber.

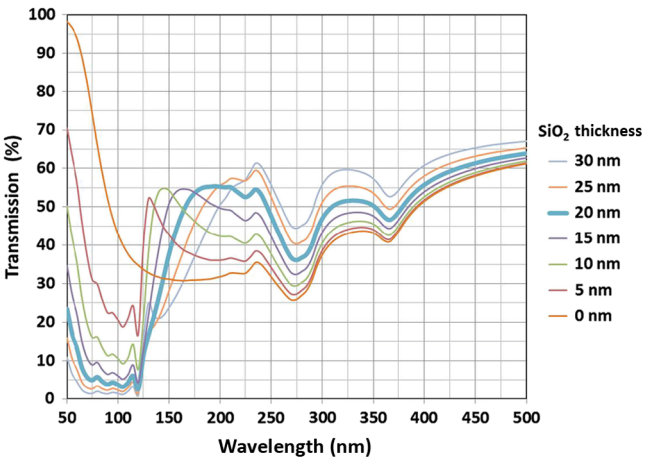

Fig. 5 Optical transmission into silicon for a SiO_2/Si system with various thicknesses of SiO_2 coating. These transmission values define an upper limit QE. An SiO_2 thickness of 20 nm (blue) and doped layer thickness of 10 nm are used in our initial study and could provide QE >50% over much of the 100 to 200 nm bandpass. The devices measured in an earlier study[2,3] had an oxide thickness of ~25 to 30 nm for comparison. This thickness could be tailored in future developments according to specific performance requirements as a function of wavelength (e.g., rejection of geocoronal Lyman-α for low Earth orbit astrophysics applications).

depth of far-UV photons in silicon (Fig. 3) fundamentally necessitates shallower doped layers in order to enhance the collection of the signal charge carriers generated by UV photons. A model of the transmission into the Si surface through different thicknesses of the Sb-doped MBE layer was utilized to calculate the internal QE (internal electrical loss). Preliminary results suggested a desired doping of 1e20 cm^{-3} and a layer thickness of $\leq$20 nm to obtain a well-passivated surface. Figure 5 shows the modeled optical transmission into silicon at various SiO_2 layer thicknesses. These transmission values also define an upper limit QE that can be achieved with single-layer SiO_2 coatings. A SiO_2 thickness of 20 nm (blue) could provide QE >50% over much of the 100 to 200 nm bandpass. Below the wavelength of ~120 nm, SiO_2 material exhibits a strong optical absorption. Additional modeling with respect to decreasing the relative efficiencies at longer wavelengths might help to limit the effects of red-leak characteristics within future instrument designs.

Prior to growth on simulated device wafers from TIS (i.e., wafers physically similar to actual device wafers but without the necessary implants to function), various experimental runs were completed on blank silicon wafers. The resulting dopant activation rate, crystallinity, and conductance were monitored for a range of target doping concentrations (3.3e18 cm^{-3}, 1e19 cm^{-3}, and 1e20 cm^{-3}), growth temperatures (350, 400, and 450°C), and epitaxial silicon thicknesses (5, 10, 16, and 20 nm). Through these experiments, it was found that in order to achieve sufficient conductance at 10 nm thickness, the target doping level had to be $\geq$1e20 cm^{-3}. At a target doping of 1e20 cm^{-3}, it was calculated from the measured conductance that ~25% of the doping layer was activated at 450°C. The SIMS study on the sample (see Fig. 7) showed that surface segregation[9] is the cause of low dopant activation. To keep more of the dopant in the film, low growth temperatures (<450°C) are preferred. However, the crystallinity of the epitaxial film was found to degrade significantly below 400°C, making 400°C the optimum growth temperature. Through this initial set of preliminary experiments reported in Table 2, the growth condition for the first batch of simulated device wafers in our next step was chosen to be 10 nm thick MBE at 1.25e20 cm^{-3} with an Sb growth temperature of 400°C.

Prior to processing the TIS wafers at LL, vapor phase decomposition (VPD) analysis was done on one of the wafers to characterize contamination levels. No gold contamination was detectable and contamination levels for other monitored metal elements were low, permitting subsequent processing in the silicon device clean rooms at LL. Metallic contamination is of primary concern for the facility, as high-quality CCDs are fabricated in the same chamber.

Several different preparation steps were performed on different wafers within the set to determine the most essential steps for controlling the quality of the wafer MBE processing. Table 3 reports the results from these 10 nm thick MBE at 1.25e20 cm^{-3} samples. Prior to MBE growth, the thinned wafers from TIS were cleaned in a variety of ways, as listed in Table 3. Etching and cleaning techniques prior to the MBE Sb-layer doping included hydrofluoric acid (HF) dip and Piranha ($H_2O_2 + H_2SO_4$), and a VPD analysis preparation (HF vapor +HF droplet). Figure 6 describes the RHEED analyses from several wafers in the test set. Inspection of RHEED imaging shows that a wafer processed using all three of these steps (w6) has the sharpest diffraction features. The measured film quality was also the best for w6. Its calculated Sb activation fraction of 26% (Table 3) is a good start, but would benefit from further optimization work. Further MBE doping and activation testing is pending, including the addition of a post-MBE H_2 sintering step.

Table 2 Electrical four-point resistivity measurements as a diagnostic of dopant activation for 20 nm thick Si:Sb films grown on p-type silicon wafers.

Wafer #	Growth T (°C)	Sb T (°C)	Doping (cm^{-3})	Thickness (nm)	Sheet-R (Ω/sq)	StDev (%)	Activated (cm^{-3})
W11	400	265	1.0e19	20	3723	11.0	7.1e18
W12	400	250	3.3e18	20	6131	12.5	3.1e18
W13	450	265	1.0e19	20	4947	4.23	4.5e18
W14	450	295	1.0e20	20	1316	9.5	2.6e19

Table 3 Electrical four-point resistivity measurements as a diagnostic of dopant activation for 10 nm thick Si:Sb films grown on thinned TIS wafers.

Wafer #	Growth T (°C)	Doping (cm^{-3})	Thickness (nm)	Sheet-R (Ω/sq)	StDev (%)	Activated (cm^{-3})	Clean
W2	400	1.25e20	10	39,618	67.6	3.4e17	HF
W3	400	1.25e20	10	3292	39.5	2.0e19	HF
W4	400	1.25e20	10	4682	13.3	1.4e19	Piranha+HF
W5	400	1.25e20	10	4148	15.0	1.6e19	Piranha+HF
W6	400	1.25e20	10	2115	4.0	3.2e19	Vapor phase decomposition & Piranha+HF

4 UV-Optimized Silicon Imaging Array Development Results

We completed detailed analyses on the process for doping thinned silicon PIN wafers with Sb, which is the key innovation needed to further enhance the UV-optimized TIS devices for science applications in the far-UV (100 to 200 nm) bandpass. As mentioned, the standard process at LL has been MBE of boron-doped Si on CCD imagers, so this represented a significant departure from established technology. Key achievements to date for the present study include the following: (1) a dozen silicon test wafers were fabricated by TIS, and shipped to and accepted by LL for MBE process setup; (2) preliminary far-UV detector QE simulation runs completed by TIS to aid MBE layer design validated the concept for UV optimization using a 20 nm depth of Sb-doped MBE on the backside of silicon PIN wafers; (3) both array and discrete detector fabrication was completed through the pre-MBE step; and (4) initial testing of the MBE doping process was performed on monitoring wafers, with detailed quality assessments.

Key metrics for the future viability of this UV-optimized silicon PIN array technology include the activation of the doping material within the intrinsic layer, which increases the conductivity and alters the Fermi level of the passivation layer. Both conductivity and Fermi level are important because the former prevents charge build-up in the backside and the latter creates a field that repels signal holes from recombining on the back

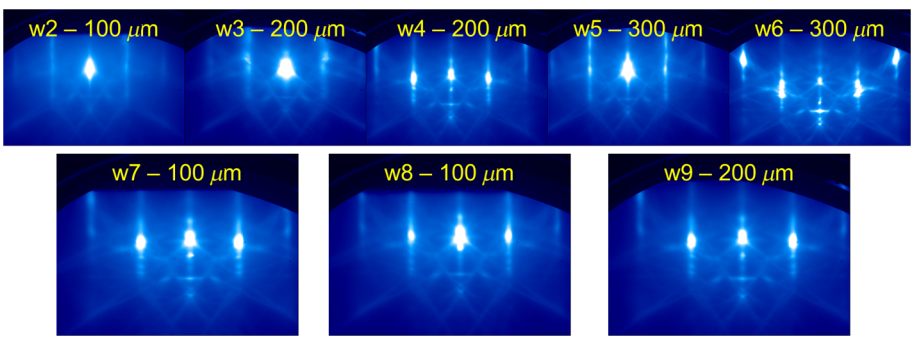

Fig. 6 Reflection high-energy electron diffraction imaging of the silicon wafers processed by MIT Lincoln Laboratory using a variety of methods to determine the best processing steps to enhance the far-UV responsivity. Top: testing of several cleaning techniques, including HF dip and Piranha ($H_2O_2 + H_2SO_4$), and a vapor phase decomposition preparation (HF vapor+HF droplet) prior to the MBE Sb-layer doping step, showed that all three steps used on w6 (at top right) worked best. Bottom: When applied to thinner wafers, more sophisticated combinations of cleaning techniques show good crystallinity prior to growth.

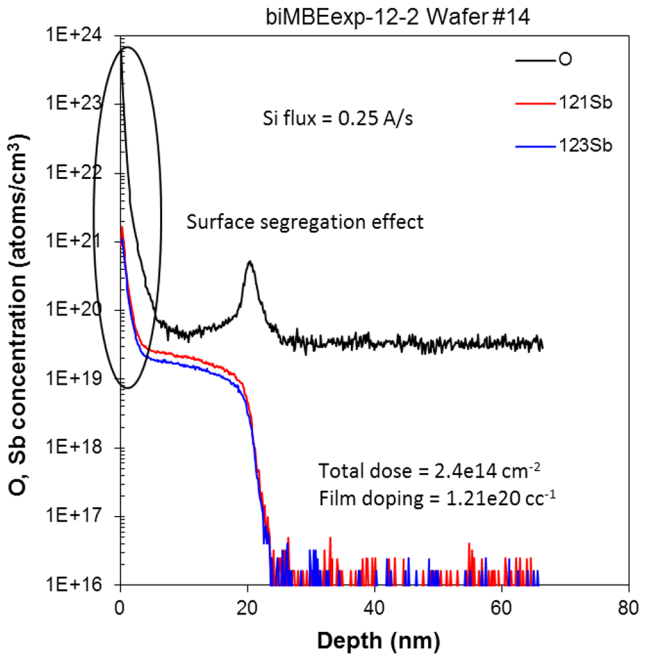

Fig. 7 Scanning ion mass spectrometry analysis of the preliminary Sb-doped MBE PIN silicon wafers indicates that an undesirable interfacial oxide layer near 20 nm depth exists (i.e., the black bump at 20 nm), but that the Sb doping in the top 5 to 10 nm depth (red and blue) is otherwise as intended.

surface. Both adequate conductivity and Fermi level must be achieved with a layer that is ≤10 nm thick and dopant concentration of >1e19 cm^{-3}. Good activation fractions of 71 and 92% have been achieved for two early-test wafers with epitaxial growth of 20 nm thick films. Higher Sb source temperatures result in a desirable sheet resistance of <2 kΩ/sq even with a thinner dopant layer thickness of ≤10 nm. While these initial results are very promising, our expectation is that additional optimization of the MBE process is achievable, based on the surface segregation effects from an interfacial oxide layer identified through the SIMS analysis shown in Fig. 7.

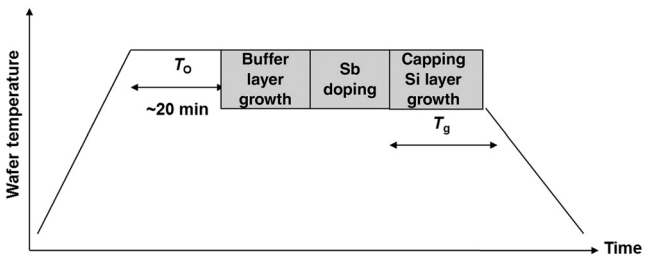

Fig. 8 To mitigate the impact of the interfacial oxide layer, an interlayer Sb-doping technique shown schematically here was briefly tested and is planned for further development.

Based on our present results, we have identified the following topics to further explore UV optimization of the devices: (1) further improvement of the wafer cleaning process prior to MBE doping to reduce process variation; (2) MBE process improvement to avoid deleterious effects from surface and interfacial oxide layers (Fig. 8); and (3) application of an H_2-sinter step after the MBE doping to further reduce the impact of native oxide on the electronic interface. The planned MBE process improvement deposits a buffer layer of pristine silicon, grown prior to the Sb-doping step, and finishes with a capping layer (<5 nm) that would prevent oxidation of the encapsulated Sb-doped layer (Fig. 8). This reduces the effects of interfacial oxide and surface segregation, thereby enabling a thinner MBE layer with good activation together with less susceptibility to surface contaminants. Table 4 shows some preliminary results of investigating this process improvement.

Our work to date has successfully applied the LL MBE process (including cleaning and etching) to TIS-provided silicon wafers as thin as 100 μm and with a diameter of 100 mm. The technical risk that these detectors would be too weak to handle the mechanical stresses and other aspects of the newly optimized manufacturing process in LL's new Veeco GEN200 chamber has been retired.

5 Summary

Encouraging progress has been made toward our primary goal of advancing the far-UV capabilities of backside-illuminated silicon PIN CMOS devices. To date, we have already demonstrated that this (previously demonstrated[9–11]) Sb-doping process applied to TIS-provided silicon wafers is feasible and provides adequate activation and electrical conduction on 100 to 300 μm thick substrates. This work included optimizing the pre-MBE wafer-cleaning process and developing a new interlayer process to improve the quality of the Sb-doped layer. After further development of the cleaning process and deposition analyses, growing films on thin wafers with silicon PIN device structures is the next step.

MBE backside-passivation remains an attractive option for high QE UV detectors and warrants further development of the Sb-doping process. Additional optimization could include testing even thinner 50 μm thick wafers and investigation of antireflection (AR) coatings that might reduce the longer wavelength red-leak background contributions. After finalizing the wafer optimization and conducting far-UV performance tests of discrete detectors, we plan to proceed to fabrication of a full detector array prototype, including hybridization to a low-noise CMOS readout chip. A detailed radiometric test

Table 4 Preliminary results of buffer layer, Sb-doped interlayer, and capping layer process. Electrical four-point resistivity measurements for 10 nm thick Si:Sb films grown on p-type silicon wafers are reported in the "Sheet-*R*" column.

Growth *T* (°C)	Buffer thickness (nm)	Doping method	Doping (cm^{-3})	Film thickness (nm)	Sheet-*R* (Ω/sq)	StDev (%)	Activated (cm^{-3})
400	5	Film	1.25e20	10	2691	41	2.5e19
450	10	Film	1.25e20	10	1780	24.5	3.9e19
450	10	Interlayer	1.25e20	10	1044	6.0	6.93e19

and characterization of the array for pixel operability, noise performance, and far-UV photon sensitivity (QE) of the final hybridized detectors would complete the study.

Acknowledgments

We appreciate the valuable input and workmanship from the teams at Teledyne Imaging Sensors (TIS) and MIT Lincoln Laboratory (LL) that conducted the wafer and molecular beam epitaxy processing needed for this project, including Desi Biasella, Ken Belanger, Joe Powers, Renee Lambert, Chris Leitz, Laurie Briere, and Julie Looney at LL, and Joseph Hosack, Raul De La Rosa, Laureen Moffett, and Edward Guerrero at TIS. This paper expands upon the 2014 report of Retherford et al.[19] We acknowledge support from NASA ROSES Planetary Instrument Definition and Development program grant NNX12AJ16G and exceptional program management from Janice Buckner.

References

1. K. D. Retherford et al., "SwRI's Alice line of ultraviolet spectrographs," *Proc. SPIE* **7441**, 744111 (2009).
2. Y. Bai et al., "Teledyne Imaging Sensors: silicon CMOS imaging technologies for x-ray, UV, visible, and near infrared," *Proc. SPIE* **7021**, 702102 (2008).
3. M. W. Davis et al., "Far ultraviolet sensitivity of silicon CMOS sensors," *Proc. SPIE* **8453**, 845308 (2012).
4. M. W. Davis et al., "Improved ground calibration results from Southwest Research Institute Ultraviolet Radiometric Calibration Facility (UV-RCF)," *Proc. SPIE* **9144**, 914433 (2014).
5. S. Nikzad et al., "Direct detection of 0.1–20 keV electrons with delta doped, fully depleted, high purity silicon p-i-n diode arrays," *Appl. Phys. Lett.* **89**(4), 182114 (2006).
6. L. R. Canfield et al., "Absolute silicon photodiodes for 160 nm to 254 nm photons," *Metrologia* **35**, 329 (1998).
7. J. W. Beletic et al., "Teledyne Imaging Sensors: infrared imaging technologies for astronomy and civil space," *Proc. SPIE* **7021**, 70210H (2008).
8. M. Loose et al., "The SIDECAR ASIC: focal plane electronics on a single chip," *Proc. SPIE* **5904**, 59040V (2005).
9. J. Blacksberg, M. E. Hoenk, and S. Nikzad, "Ultra-low-temperature homoepitaxial growth of Sb-doped silicon," *J. Cryst. Growth* **285**(4), 473–480 (2005).
10. J. Blacksberg et al., "Enhanced quantum efficiency of high-purity silicon imaging detectors by ultralow temperature surface modification using Sb doping," *Appl. Phys. Lett.* **87**, 254101 (2005).
11. J. Blacksberg et al., "Near-100% quantum efficiency of delta-doped large-dormat UV-NIR silicon imagers," *IEEE Trans. Electron. Devices* **55**(12), 3402–3406 (2008).
12. B. C. Jacquot et al., "Characterization and absolute QE measurements of delta-doped N-channel and P-channel CCDs," *Proc. SPIE* **7742**, 77420I (2010).
13. T. J. Veach et al., "Modified modular imaging system designed for a sounding rocket experiment," *Proc. SPIE* **8446**, 84467F (2012).
14. M. E. Hoenk et al., "Superlattice-doped silicon detectors: progress and prospects," *Proc. SPIE* **9154**, 915413 (2014).
15. R. C. Westoff et al., "Low-dark-current, back-illuminated charge-coupled-devices," *Proc. SPIE* **7249**, 72490J (2009).
16. E. D. Palik, *Handbook of Optical Constants of Solids*, Vol. 3, University of Maryland, College Park, Maryland (1998).
17. B. E. Burke et al., "CCD imager technology development at Lincoln Laboratory," in *Optical Detectors for Astronomy II*, P. Amico and J. W. Beletic, pp. 187–199, Kluwer Academic Publishers, The Netherlands (2000).
18. R. E. Honig and D. A. Kramer, "Vapor pressure data for the solid and liquid elements," *RCA Rev.* **30**, 285–305 (1969).
19. K. D. Retherford et al., "Enhancing the far-UV sensitivity of silicon CMOS imaging arrays," *Proc. SPIE* **9154**, 915412 (2014).

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