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HIGH PERFORMANCE UV/VISIBLE MICROCHANNEL PLATE DELAY LINE DETECTOR TECHNOLOGIES

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ABSTRACT *We have pioneered the development of the first delay line image readout systems for high resolution, large format, photon counting MCP detectors in space instrumentation for satellite (SOHO [Siegmund 94], FUSE, IMAGE), rocket [Sarlin 94], and shuttle payloads (ORFEUS) [Hurwitz 91]. We are currently developing the next generation of delay line detectors with enhanced performance characteristics. These include high spatial resolution ($<15\mu\text{m}$ FWHM) and linearity, high image stability with low fixed-pattern noise, low power consumption and weight, and large image formats ($\approx 170\text{mm} \times 10\text{mm}$ cf. FUSE) with high encoding rates ($>1\text{MHz}$). We have developed planar and multilayer double delay line, and crossed delay line anodes that are compact and robust, and allow considerable flexibility of design and optimization.*

1 - INTRODUCTION

Microchannel plate (MCP), photon counting detectors are being used with great success on many NASA and ESA missions in the $100\text{\AA} - 3000\text{\AA}$ range. These include the ROSAT, EUVE, ALEXIS, ORFEUS-SPAS, HST STIS and SOHO (CDS, UVCS & SUMER) (Fig. 1). MCP detectors have also been chosen to fly on future missions such as IMAGE (Fig. 2), FUSE (Fig. 3), FUVITA, ROSETTA, HST-COS and GALEX. In recent years we have begun to design microchannel plate detectors employing delay line image readout schemes for many of these space applications. Many delay line detector formats and types are possible, and include the double delay line (DDL) [Lampton 87, Siegmund 89], the multiwire wound helical delay line [Williams 89], and the crossed delay line (XDL) [Siegmund 94, Friedman 96] schemes. In general the planar and multilayer designs are compact and robust, have high performance imaging, and allow considerable flexibility of design and optimization.

The design of a delay line anode MCP detector system is essentially similar to many other photon counting MCP sensors (cf. wedge and strip, resistive anode). A MCP stack with two or three MCP's detects the incoming photons and multiplies the charge signal. The resulting charge cloud is accelerated over a gap (a few mm) and deposited onto the readout anode. Typical charge clouds are $\approx 1\text{mm}$ in size and are deposited onto the anode in a few ns. Delay line schemes encode the photon event position centroids in one, or two, axes by determination of the difference in arrival time of the event signal at the two ends of a conductive transmission line anode. In each dimension the centroid (X_c or Y_c) position of a photon event is given by, $X_c = (T+T_d)V/2$, where, V is the characteristic velocity of signal propagation, T is difference in signal arrival times, and T_d is a fixed delay. T varies from $-t$ to $+t$, where t is the overall end to end delay of the anode (T_d is set at $\approx t$ to normalize the coordinates). Depending on the design the single pass delay can be in the range from 10ns to 200ns. Encoding electronics can be a variety of designs, but a typical scheme consists of high bandwidth amplifiers for each anode end, followed by timing discriminators. These signals provide start & stop for a time to amplitude converter (TAC), the output of which is converted with an analog to digital converter (ADC) to give the event centroid coordinate.

Specific examples of delay line detector systems include the XDL detectors (Fig. 1) are currently in operation on the SOHO (UVCS and SUMER) satellite. These have a $25\text{mm} \times 9\text{mm}$ active area encoded with a $33 \times 15\text{mm}$ multiplanar XDL anode design, and are designed for operation up to 500 kHz rates. A similar design is also used for the IMAGE satellite Spectrographic Imager (SI) detectors (Fig. 2). These have a $22 \times 22\text{mm}$ active area encoded by a $27 \times 27\text{mm}$ XDL anode at rates up to 100 kHz. One of the most challenging detector designs (Fig. 3) is that for the FUSE satellite. Here two cylindrically curved MCP detector segments (each $88.5\text{mm} \times 10\text{mm}$) are encoded with two cylindrically curved double delay line anodes (each $94\text{mm} \times 15\text{mm}$) at rates of up to 40 kHz with $\approx 4500 \times 200$ resolution elements each.

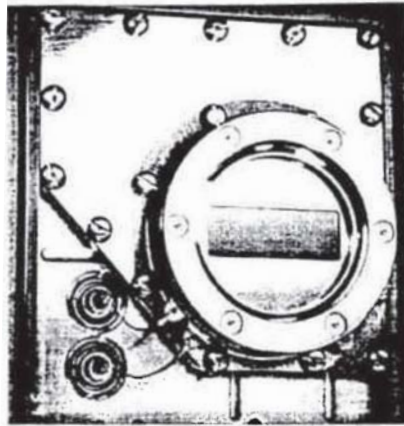


Figure 1. SOHO XDL microchannel plate detector, 25mm x 10mm active area.

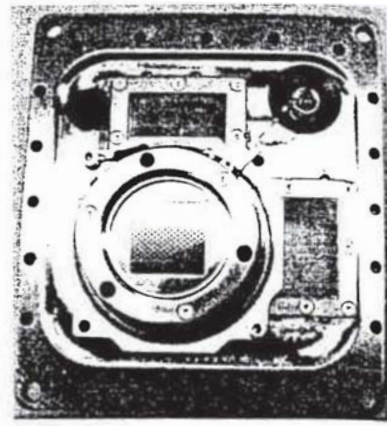


Figure 2. IMAGE Spectrographic Imager XDL microchannel plate detector, 22mm x 22mm

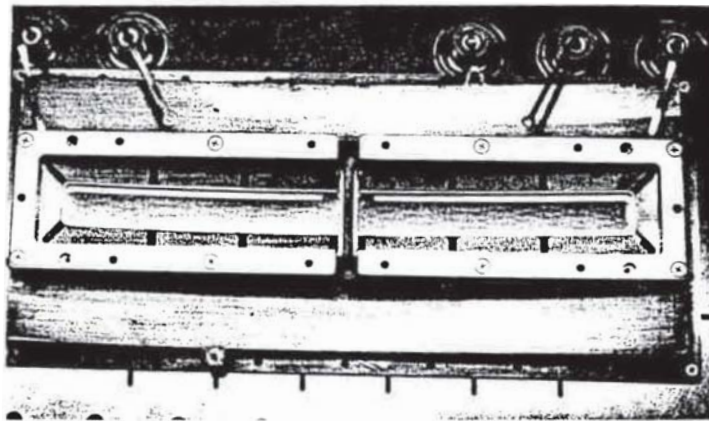


Figure 3. FUSE DDL microchannel plate detector with two 85mm x 11mm, cylindrically curved, MCP segments

2 - DELAY LINE ANODE SCHEMES

2.1 - Double Delay Line Anodes

One of the most basic anode designs is the DDL (Fig. 4). The MCP charge pulse ($\approx 3-5$ ns width) is detected on, and divided between, two sets of conductive wedges, so that the Y event centroid coordinates may be determined from the ratios of charge signals on the opposing wedge sets ($Y = Q_a / (Q_a + Q_b)$). The wedges are connected to external serpentine delay lines [Siegmond 89] (not shown in Fig. 4) so that the pulse arrival time at each end of the delay line is a linear function of the X position of the original event. Planar DDL's are produced by photolithographically etching the anode pattern into a conductor layer deposited on a low loss microwave substrate. The anode substrates can be RT/Duroid (ceramic doped PTFE, $\epsilon_r \approx 10.5$, loss coefficient 0.0023 @ 10 GHz, 250 μ m thick) or alumina, coated with Cu or gold on both sides (delay plane & ground plane). The high dielectric constant and the length of the delay line serpentine slow down the pulse propagation speed so that typical scale factors are in the range ≈ 1 ns/mm. Double delay line anodes are convenient for applications in spectroscopy, where the spectral encoding axis requires high resolution, but the cross-dispersion axis is less demanding. DDL anodes with RT/Duroid substrates are also capable of being bent into various shapes to accommodate applications such as FUSE. Long DDL formats can be accommodated, but care must be taken in the anode design to minimize the attenuation and dispersion of signals travelling across large distances on the anode. Anodes of this type have been flown on several rocket [Sarlin 94] and shuttle missions [Hurwit: 91].

To obtain large readout formats with the highest spatial resolutions we have developed the helical double delay line anode (HDDL). The HDDL anode scheme also splits the MCP charge between two wedge sets (Fig. 4). However, instead of a planar serpentine delay line, the anode has external helical delay lines. Half of each external delay loop is on the top surface of the substrate, and the other half is on the back side of the substrate (Fig. 4). A ground plane is introduced between the layers to prevent crosstalk. The top and bottom delay line conductors are connected, period to period, by plated through holes in the composite substrate. The delay line propagation speed for HDDL anodes is typically ≈ 2 ns/mm due to the greater pattern frequencies achievable, and the transmission line configuration. Assuming electronics with the same time resolution limit, this provides better spatial resolution than DDL anodes. Most recently we have been using a 94mm x 15mm multiplanar HDDL design optimized for spectroscopy (FUSE), with a 0.44mm period, and double pass delay time of ≈ 210 ns giving a scale of 2.2ps μ m⁻¹.

Delay lines of this type are also produced by a photolithographic etch methods. The upper delay line and wedge patterns are etched into the copper surface of the top Duroid substrate. Then the mid ground plane and bottom delay line are etched on separate Duroid substrates (≈ 0.005 " thick). All three layers are then aligned and bonded together and contacts between layers are established using plated through holes.

Although both DDL and HDDL anodes have the potential for high counting rates, the limitation is set by the Y dimension encoding by the charge division electronics. To obtain high Y resolution the noise in the charge amplifiers is minimized by using long (1μ s) pulse shaping time constants, thus rates greater than 100 kHz are difficult to obtain while maintaining high Y axis resolution.

2.2 - Cross Delay Line Anodes

For high speed two dimensional imaging detectors we have designed multilayer monolithic crossed delay line anode schemes. These have two orthogonal sets of fingers in the charge collection area (Fig. 5, 6). The fingers in each axis are connected to "external" serpentine delay lines etched onto Cu on a high dielectric constant base substrate. Since there is no charge division encoding, and the anode propagation times are usually from 10ns to 100ns, very high counting rates may be accommodated (> 1 Mhz). The XDL scheme allows the ratio of finger widths, and the size of the active area to be varied independently from the delay line, and the layer stackup to be kept thin (< 0.010 ").

Design and fabrication strategies vary, but usually both serpentine external delay line patterns, and one set of fingers (X), are etched into copper on the base substrate. Photo-imageable polyimide is then applied, imaged and cured to give a set of fingers orthogonal to the fingers on the base substrate. Metal fingers are applied to the polyimide fingers using sputtering, liftoff, etch back and plate up processes to add a ground plane finger set between X and Y planes. The polyimide/metal process is then repeated to complete the second encoding axis. Anodes of this type with alumina ceramic substrates have been built and tested (up to 65 x 65mm), and provide

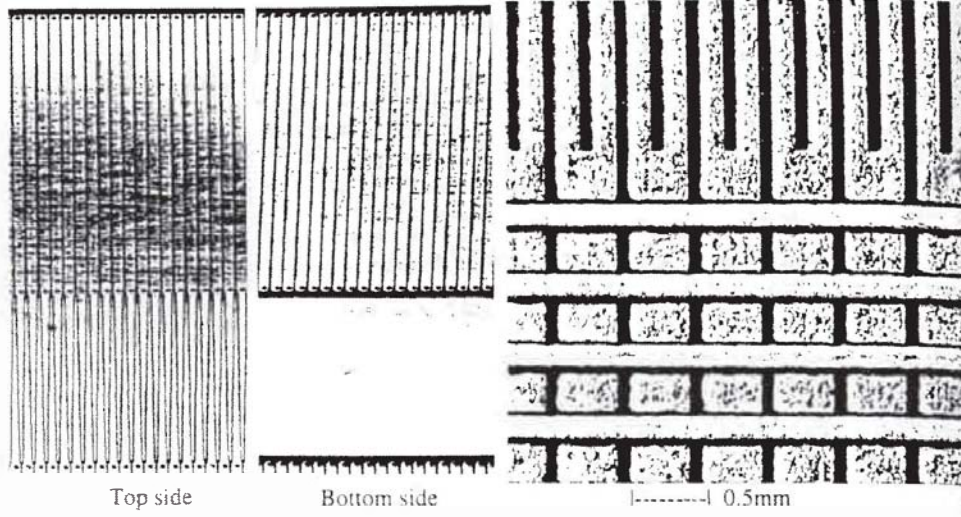


Figure 4. Segment of a FUSE helical DDL anode with interleaved wedges in the active area & helical delay lines connected by plated through holes.

Figure 5. Segment of an XDL anode (Fig. 6.) showing the X and Y charge collection fingers & the X delay line serpentine.

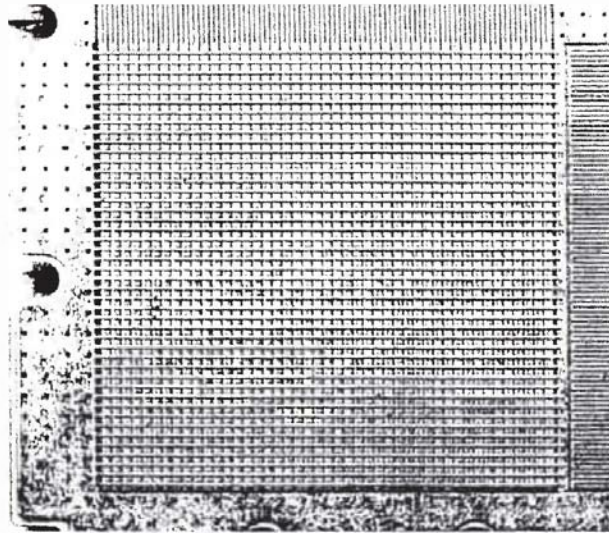


Figure 6. Cross delay line anode for IMAGE S1 detector, showing the 27mm x 27mm active area and part of the X & Y delay line serpentes

$\leq 25\mu\text{m}$ X & Y resolution with good stability and linearity [Siegmund 94, Siegmund 93] and were used successfully on four SOHO satellite detectors (32 x 15mm anode format).

The polyimide technique is not best suited to ultra high vacuum applications, such as visible photocathode sealed tube devices. Therefore we have developed an alternative fabrication technique for compatible XDL anodes. The copper delay lines and one axis set of fingers are patterned on a ceramic substrate (Al_2O_3 , $\epsilon_r \approx 10$) using copper. Then the insulator, conductor, insulator, conductor fingers are applied, but using a ceramic insulating material. Since all materials are refractory this produces a highly clean, robust, anode suitable for sealed tubes. This type of anode has been produced for the IMAGE SI detectors (Fig. 5, 6) (27 x 27mm anode format), and shows good repeatability and pattern accuracy.

3 - DELAY LINE POSITION ENCODING ELECTRONICS SCHEMES

3.1 - Time, to amplitude, to digital position encoding

A position encoding electronics scheme for DDL anodes is shown schematically in Fig. 7. The X position encoding electronics uses a fast timing amplifier at each anode end, which contains a low pass filter ($\approx 120\text{MHz}$) to optimize the pulse shape and signal to noise ratio. The fast timing amplifier signals are detected by constant fraction discriminators (CFD) (50% fraction) which produce timing signals for start and stop. One signal is delayed, using a lumped delay module, to ensure the "start" pulse always precedes the "stop" signal. The time difference between these "start" and "stop" signals are converted to analog voltages by a time to amplitude converter. Then the analog voltage pulses are digitized by an analog to digital converter to provide the photon centroid position. The differential non-linearity (DNL) of typical ADC's cause variations ($\pm 50\%$) in the width of the least significant bit. This is solved by using a digital "dither" by adding a known voltage to the ADC input & then digitally subtracting it at the ADC output. Since the voltage is varied from event to event this has the effect of averaging the ADC DNL over a number of channels. Maximum resolution is achieved by appropriate selection of ADC's such that the electronic binning in X oversamples ($> \times 3$) the intrinsic detector point spread function.

The Y axis encoding electronics has charge sensitive preamplifiers followed by gated integrator shaping amplifiers. The gated integrators provide a short dead time and no loss of spatial resolution at the higher counting rates, compared with conventional bipolar shaped amplifiers. The Y event centroid coordinates are determined by digitization of the gated integrator signals and a subsequent hardware (or software) sum and divide. In the case of FUSE, the X axis is digitized to 14 bits ($\approx 6\mu\text{m}$), and Y to 10 bits ($\approx 10\mu\text{m}$). Y resolution is predominantly determined by the signal to noise ratio, primarily set by the capacitive load on the charge amplifiers. The resolution in the delay line axis in this system is determined by the event timing error. This is dominated by the CFD jitter and walk, & noise in the TAC, which are typically of the order ≈ 8 to 10ps FWHM total.

Position encoding for XDL anodes simply uses two sets of the DDL X axis encoding electronics (7w per axis). This was implemented for the SOHO XDL [Siegmund 94] detectors using 12 bit ADC's (1.3 μs settling time) for each axis. This allowed random counting rates of up to 500 kHz to be accommodated (Fig. 8, 40% dead time) without significant effects on the position resolution. Higher rates could be accommodated with faster ADC's, but there is a penalty in greater power consumption and in degraded resolution at high rates due to finite reset times for the TAC's. Therefore we have developed a different scheme for position encoding that draws less power and with higher rate capability.

3.2 - Time to digital position encoding

We have been developing high speed electronics to encode event positions, in particular, with the XDL scheme readout anodes. To achieve both high resolution and speed we have commissioned a high speed arctangent time to digital converter [Lampton & Raffanti, 1994]. This scheme converts the delay line signal times of the start to stop signals in each axis from clock signal timing. Four derived clock signals are used, slow (6.25 MHz) sine and cosine waves and fast (200 MHz) sine and cosine signals. Digitization of both slow signals (to 8 bits) at the start and stop times give a coarse position from the difference in signal phase. The fine position is then derived similarly from the digitization (12 bit, 40MHz ADC) of both fast signals. The hardware dead time is primarily set by the settling time of the sample/hold amplifier used to sample the fast (200 MHz) sinusoids prior to analog/digital conversion, and by the propagation delay of the anode. The former is about 50ns, so for most applications the anode delay time dominates the system dead time. This electronics has a deadtime loss of $\approx 10\%$ at count rates of 1 MHz, and shows no degradation of resolution at that rate. Use of a FIFO following the analog/digital

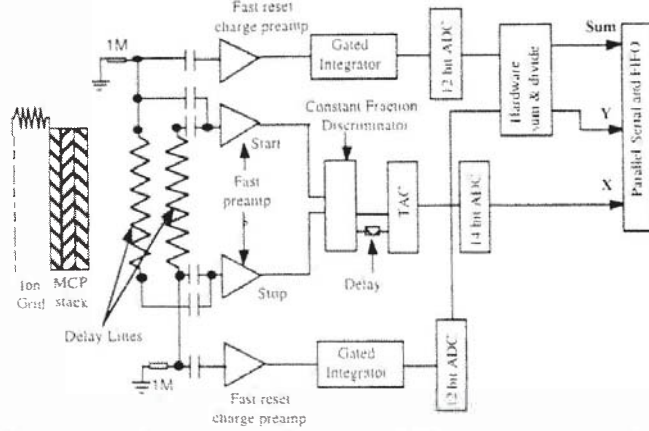


Figure 7. DDL event position encoding electronics (time - amplitude) block diagram

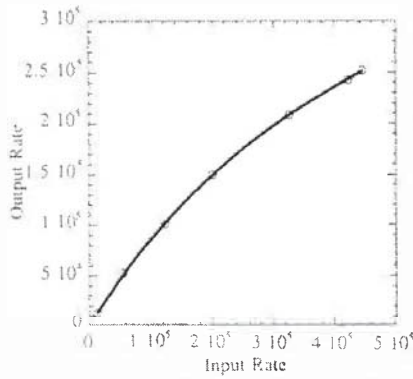


Figure 8. Counting rate throughput for the SOHO XDL electronics based on CFD/TAC/ADC's

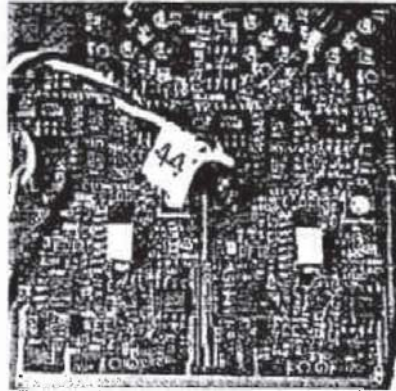


Figure 9. Layout of high speed interpolation delay line position encoding electronics.

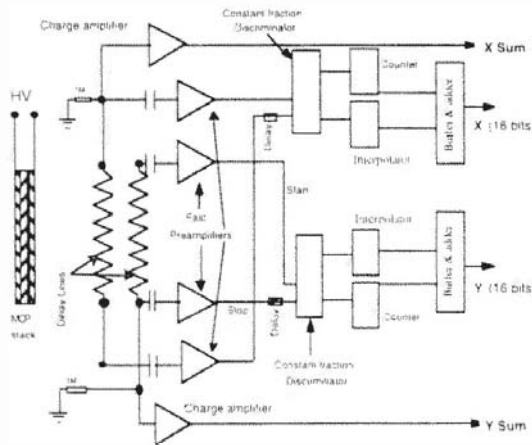


Figure 10. High speed XDL event position encoding electronics block diagram

conversion evens out digital event data flow, and optimizes the dead time performance. Resolution of the current breadboard is ≈ 5 ps rms, which is slightly worse than the 3ps rms for conventional CFD/TAC/ADC systems we have used on flight systems (ORFEUS, SOHO). In tests with a 65mm x 15mm DDL anode detector system the arctangent electronics achieved the same resolution ($< 25\mu\text{m}$ FWHM) as the standard electronics. One disadvantage of this scheme, however, is that the power increases to $> 10\text{w}$ per axis.

A second generation of time to digital high speed encoding electronics has now been built. This electronics utilizes the scheme of counting high frequency clock cycle intervals for coarse position and interpolation of phase shift delays for fine positions. The scheme uses the same amplifiers as the previous designs, but has different CFD's feeding new counter, interpolator and digital logic algorithm circuits (Fig. 10). We have created circuit board designs using surface mount components, thus reducing the board size significantly (Fig 9). The overall board size is $\approx 18\text{cm} \times 9\text{cm}$, which accommodates the electronics for both axes if both sides of the board are used. The power requirement is 3 to 5w for each axis, depending on the ADC's chosen, and the least significant bit timing accuracy is $\sim 1\text{ps}$ to allow point spread function oversampling. 3MHz, 8MHz and 10MHz 14 bit ADC configurations have been built, which will allow event rates of several MHz to be achieved with up to 24 bit X and Y coordinate digitization. Even higher event rates could be accommodated by using faster (40MHz) 12 bit ADC's assuming a reduction of the number of output bits.

4 - DELAY LINE DETECTOR IMAGING PERFORMANCE CHARACTERISTICS

4.1 - Image linearity and resolution

Evaluation of the imaging performance of delay line detectors is often accomplished by imaging arrays of small pinholes illuminated with UV light. This type of test image is shown in Fig. 11 for a XDL MCP detector with a 27mm x 27mm all ceramic anode. This anode has $\approx 15\text{ns}$ single pass delay, and is encoded with an amplifier, CFD/TAC/ADC electronics system with 16 bit digitization. Measuring the position and the FWHM of the pinhole images allows the linearity and resolution of the detector to be assessed. The image array in Fig.11 is almost distortion free, with both axes closely orthogonal to each other ($90^\circ \pm 0.5^\circ$). The detector configuration for delay line anodes places the anode a few mm behind the MCP stack, and the anode is usually a few mm wider than the required field of view. Under these conditions the charge cloud dimensions are usually uniform, thus providing stable image linearity and resolution characteristics. Typical resolution with XDL anodes is of the order $25\mu\text{m}$ FWHM for our conventional encoding electronics. The images of the pinhole point spread functions in Fig. 12, show some of the better results at a digitization of $\approx 4\mu\text{m}/\text{bin}$ using a 65mm x 15mm XDL anode. The resolution is not signal to noise limited at the MCP stack gain levels we usually employ ($\approx 1 \times 10^7$), but rather by the by the fixed contributions of CFD jitter, and noise in the TAC. At resolution levels of $\approx 20\mu\text{m}$ the MCP pores ($10\mu\text{m}$ to $12\mu\text{m}$) can also be a significant impact to the resolution. Lastly, amplitude walk in the discriminators can be a source of blur, however it is usually possible to trim the electronics to null out walk. Thus it is possible to operate the detector without degradation of the position resolution over a wide range of MCP gains.

For large detector anodes (cf. FUSE) we have used HDDL designs, rather than DDL's, to achieve better resolution by virtue of the increased delay time per unit length. The large anode formats require the consideration of the signal attenuation and dispersion, which are not very important for the smaller format anodes ($< 30\text{mm}$). Pulse widths on the FUSE HDDL 94 x 15mm anodes increase to $\approx 7\text{ns}$ wide, and there is a substantial broadening and attenuation of the pulses as they originate at greater distances from the anode contacts. Nevertheless, using the electronics scheme of Fig. 7 resolution of $\approx 20\mu\text{m}$ is achieved in tests using $10\mu\text{m}$ pore MCP stacks, with some degradation of resolution towards the anode ends. A histogram of all the resolution data (Fig 14) shows that the peak is $\approx 20\mu\text{m}$ FWHM with a tail towards larger values due to the resolution decrease at the anode ends. The position linearity is evaluated by determining the difference of the pinhole image positions from assumed perfect grid positions. The deviations are somewhat random and generally better than ± 1 resolution element over most of the detector field of view (Fig. 15). However, there are also $\pm 5\mu\text{m}$ errors in the fabrication of the pinhole mask and the relative position of the $10\mu\text{m}$ pores in the MCP's introduces another source of error. Thus the intrinsic overall differential image non-linearity of HDDL anodes is very low.

When the ($10\mu\text{m}$) pinholes are carefully placed so as to line up with individual MCP pores, the fundamental limit of the readout is more clearly assessed. In Fig.16 three pinholes are seen virtually lined up with the pores. Since the electronics timing error (8 - 10ps FWHM) remains



Figure 11. Image section of a 2 x 2mm, 10µm pinhole mask imaged on a 27mm² XDL detector.

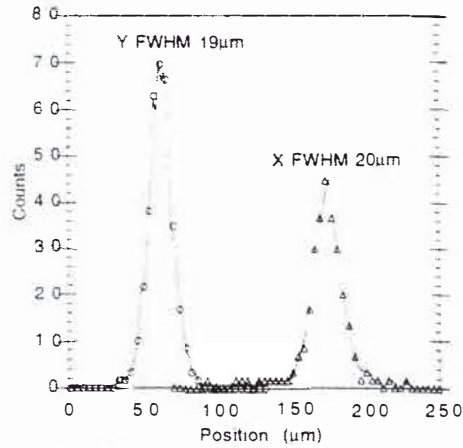


Figure 12. X & Y histograms of a 10µm pinhole image taken with a 65 x 15mm XDL.

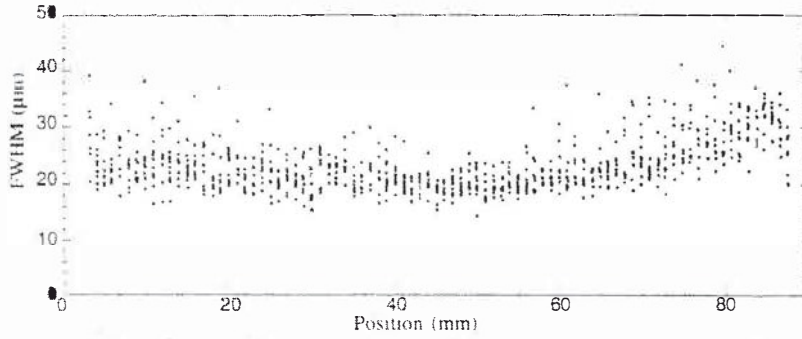


Figure 13. 10µm pinhole image FWHM v.s. X. 94 x 15mm HDDL, 10µm pore MCP stack.

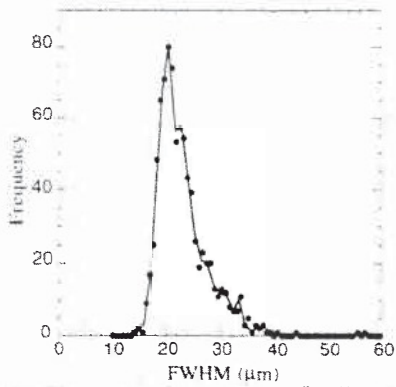


Figure 14. X resolution histogram for Fig. 13 showing the distribution of spot image widths.

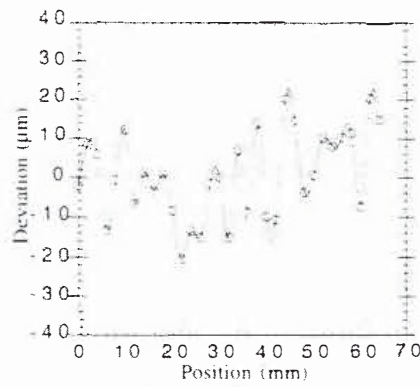


Figure 15. Image linearity as a function of X for a 94 x 15mm HDDL & 10µm pore MCP's.

essentially the same, the electronic resolution should be $\approx 5\mu\text{m}$ for the HDDL with a $2.2\text{ps}/\mu\text{m}$ scale factor. Our results show resolution of $\approx 11\mu\text{m} - 13\mu\text{m}$ FWHM (≈ 8000 resolution elements) in the 94mm axis (X). Note there is a suggestion that two pores are being illuminated in the center pinhole image. A more controlled way of probing the resolution performance is accomplish this by optically projecting [Siegmond 1993] and scanning small ($<7\mu\text{m}$) spot and slit images across the MCP to determine the position sensitivity of the anode and the quantization effect of the MCP pores on resolution. Fig. 17 shows that as the spot of light is scanned across the MCP surface the width of the spot image and its count rate oscillate. The two parameters vary exactly out of phase, the counting rate being at maximum when the resolution is at minimum. This situation corresponds to a narrow image point spread function when the spot is projected directly down a single MCP pore, maximizing the count rate. Conversely, the resolution is worst when the spot straddles two MCP pores & the count rate drops due to events being lost to the MCP web area.

With resolution of the delay line anodes so close to the pore dimensions of $10\mu\text{m}$ ($12\mu\text{m}$ center to center) we should also see the performance, particularly of the HDDL, improve with small pore MCP's ($5\mu\text{m}$, $6\mu\text{m}$ and $8\mu\text{m}$) [Siegmond 96]. An indication of what is possible is shown in Figs. 18 & 19. An Air Force 1951 test pattern (AFTP) imaged with a $10\mu\text{m}$ pore MCP intensifier achieves a limiting contrast transfer function (CTF) resolution at ≈ 36 lp/mm ($14\mu\text{m}$ line). When one of the new $6\mu\text{m}$ MCP's is substituted, the limiting CTF goes up to ≈ 57 lp/mm ($9\mu\text{m}$ line). When sufficient numbers of such MCP's are available we will evaluate the comparative resolution for delay line readout anodes.

4.2 - Fixed pattern noise

The inherent fixed pattern noise for delay line detectors can be evaluated by accumulating a "flat field" image with a large number of events at a high spatial sampling frequency. Fig 20 shows that the dominant source of fixed pattern noise is the MCP multifiber structure [Vallerga 89], provided the MCP's do not suffer from Moire fringing effects [Siegmond 97]. The multifiber modulation is about 10% and is stable, however other effects are also visible, such as dead spots (Fig. 20) in the MCP's that are often associated with particulate contamination between the multifibers occurring during MCP fabrication.

5 - ACKNOWLEDGMENTS

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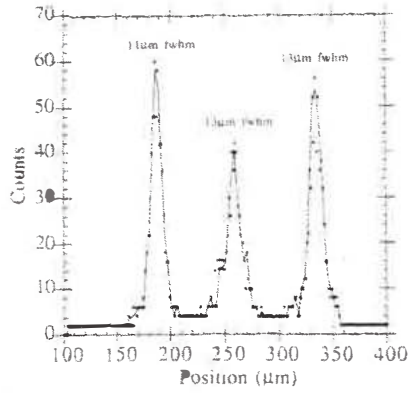


Figure 16. Point spread functions of 10µm pinhole images using a 10µm pore MCP stack and a 95mm x 15mm HDDL anode.

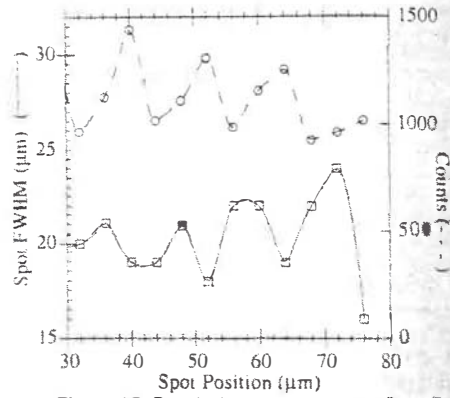


Figure 17. Resolution and count rate for a 7µm spot scanned over a 10µm pore MCP stack with a 65mm x 15mm DDL readout.



Figure 18. 1951 AFTP imaged with a 10µm pore Philips 33mm MCP in an image intensifier



Figure 19. 1951 AFTP imaged with a 6µm pore Philips 33mm MCP in an image intensifier.

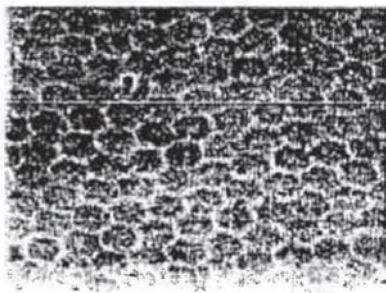


Figure 20. High resolution flat field for a 10µm pore MCP stack & a 94mm x 15mm HDDL.

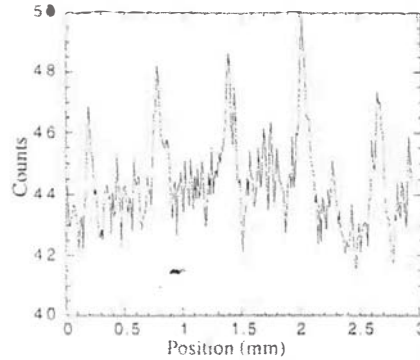


Figure 21. Histogram slice through Fig. 20, showing the periodic multifiber modulation.