International Conference on Space Optics—ICSO 2004

Toulouse, France

30 March–2 April 2004

Edited by Josiane Costeraste and Errico Armandillo

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esa icso proceedings cnes

International Conference on Space Optics — ICSO 2004, edited by Errico Armandillo, Josiane Costeraste, Proc. of SPIE Vol. 10568, 105681O · © 2004 ESA and CNES
CCC code: 0277-786X/17/$18 · doi: 10.1117/12.2307970

RESEARCH-GRADE CMOS IMAGE SENSORS FOR DEMANDING SPACE APPLICATIONS

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ABSTRACT

Imaging detectors are key elements for optical instruments and sensors on board space missions dedicated to Earth observation (high resolution imaging, atmosphere spectroscopy...), Solar System exploration (micro cameras, guidance for autonomous vehicle...) and Universe observation (space telescope focal planes, guiding sensors...). This market has been dominated by CCD technology for long. Since the mid-90s, CMOS Image Sensors (CIS) have been competing with CCDs for more and more consumer domains (webcams, cell phones, digital cameras...). Featuring significant advantages over CCD sensors for space applications (lower power consumption, smaller system size, better radiations behaviour...), CMOS technology is also expanding in this field, justifying specific R&D and development programs funded by national and European space agencies (mainly CNES, DGA, and ESA). All along the 90s and thanks to their increasingly improving performances, CIS have started to be successfully used for more and more demanding applications, from vision and control functions requiring low-level performances to guidance applications requiring medium-level performances. Recent technology improvements have made possible the manufacturing of research-grade CIS that are able to compete with CCDs in the high-performances arena. After an introduction outlining the growing interest of optical instruments designers for CMOS image sensors, this talk will present the existing and foreseen ways to reach high-level electro-optics performances for CIS. The developments of CIS prototypes built using an imaging CMOS process and of devices based on improved designs will be presented.

1. INTRODUCTION

The advantages featured by CMOS Image Sensors (CIS) for space applications have been extensively presented in previous papers (see for instance [1]-[4]). These advantages are not necessarily the same as the ones justifying the choice of CIS for consumer applications. For instance, the cost of the device could not be the main driver for space applications, as it could be negligible with respect to the cost of its packaging, its qualification and characterisation. When compared to CCDs, specific features of CIS (such as the integration of control electronics, on-chip signal processing, ...) could mainly lead to strong system advantages (easier feasibility, lower cost, reduced mass/power budgets...), as summarized by fig. 1.

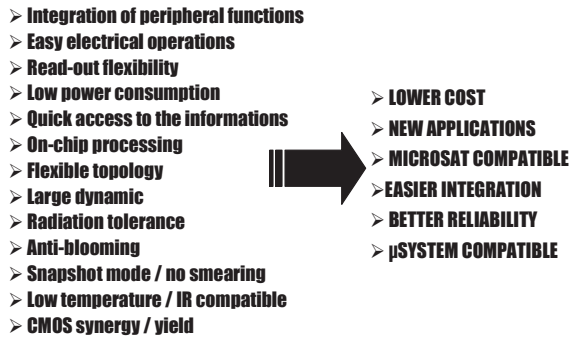

Fig. 1. CMOS image sensor characteristics lead to strong system advantages

The abilities of CIS to integrate on-chip functions which were previously peripheral to the device and to be designed in order to perfectly fit a given application were the main reasons that convinced EADS-Astrium to be in position of mastering the design of CMOS image sensors (following an "image sensor ASIC-like" approach). This is done since 1998 through an agreement with the CIMI laboratory of Supaéro (also located in Toulouse), which started to work on high performances CIS since 1994. Thanks to internal funding and the gain of agencies contracts, several devices were developed by this join-team in order to provide an efficient answer to space requirements. Fig. 2 presents a 750x750 pixels CIS specifically designed in order to fit star trackers and optical telecommunications needs.

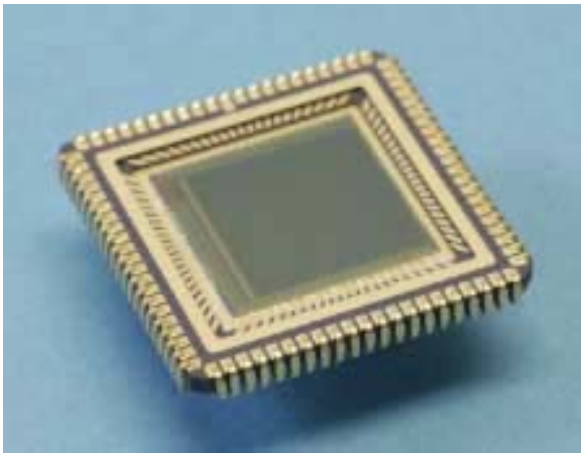

Fig. 2. 750x750 pixels CIS dedicated to Star Trackers and optical communications

This device was developed through a CNES contract. One of its most interesting features is a powerful integrated programmable timing and control function able to randomly read a large number of windows. This device was extensively characterised, featuring very good electro-optics performances and was space radiation qualified (total dose, latch-up and high energy protons). [5] presents the main performances of this image sensor.

2. THE NEED FOR ELECTRO-OPTICAL PERFORMANCES IMPROVEMENTS

Monolithic CIS developed by both EADS-Astrium and Supaéro-CIMI in the 1998-2002 period are featuring very good electro-optical performances, close to the ones achieved by standard front-side illuminated CCDs. Table 3 summarizes typical performances that were measured when testing CIS in our laboratories.

Table 3: typical electro-optical performances reached by EADS-Astrium/Supaéro-CIMI CIS 2D arrays

Parameter	Typical figure
Photodetector	Photodiode/PhotoMOS
Peak detection efficiency	30-40% (∩ Fill Factor)
Photo Response Non Uniform.	< 1% std dev.
Read-out noise (rms)	<200µV @ 4Mpixels/s
Dynamic	75dB linear/80dB total
Conversion factor	1 to 30 µV/e-
Dark current	0.5-1 nA/cm^2 @25°C
Dark Signal Non Uniform.	5-10% std dev.
MTF @Nyquist (500 nm)	0.45 row / 0.55 column

With such characteristics, and thanks to their numerous advantages over CCDs, monolithic CIS manufactured using standard CMOS technologies are today the good solution for several space applications, such as Star Trackers, Optical Communications, miniature scientific cameras....

On the other hand, some of these electro-optical performances are not sufficient in view of allowing CIS to compete with scientific CCDs for very demanding applications such as high resolution Earth Observation and scientific instruments operated in low flux regime. In addition, the continuous decrease of modern CMOS process design rules would lead to a continuous decrease of the thickness of the interaction layer between photons and silicon, resulting at least in a detection efficiency decrease (particularly for the longest wavelengths) and a loss of MTF (part of the

carriers being created in the substrate and being diffusion collected by the neighbouring pixels).

3. POSSIBLE WAYS TO IMPROVE CIS ELECTRO-OPTICAL CHARACTERISTICS

At least three ways can be foreseen to improve the electro-optical performances of CIS. All of them are described below taking into account that the first one is non exclusive with the two others, while the second and the third ways cannot be mixed together.

3.1 Improvements by design

For a fabless company, the easiest way to improve CIS performances is to optimise its design, and particularly the intra-pixel circuitry. [6] and [7] describe for instance new photodiode pixel architectures offering kTC noise reduction. EADS-Astrium and Supaéro-CIMI are investigating pixel designs expected to improve important parameters for Earth Observation such as spectral quantum efficiency, MTF, read-out noise and linearity at low flux. A study awarded by CNES to EADS has allowed producing a test vehicle dedicated to these investigations (see Fig. 4). This device will be tested in 2004.

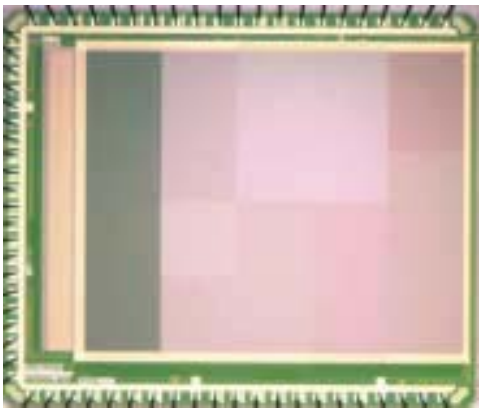

Fig.4: test vehicle built through an R&T CNES contract in order to improve pixel performances using standard CMOS technologies

In collaboration with CEA/LETI, a study awarded by DGA to our team has allowed evaluating the CMOS technology capabilities for very large focal planes dedicated to Earth Observation (both linear and TDI devices architecture being investigated). Fig. 5 presents an example of linear array design with CTIA injection stage implemented at pixel level, allowing image acquisition at high frame rate even for very low flux conditions.

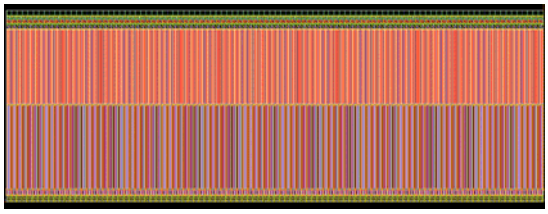

Fig. 5: layout of a linear array with CTIA injection stages devoted to pushbroom Earth observation

3.2 CMOS technology improved for Imaging applications

The second way that can be used to get better CIS performances is the improvement of CMOS mixed signal process in view of offering specific features useful for imaging applications (see [8]). The main parameters that request improvements are the dark current, using specific technological processes of the wafers, and the quantum efficiency plus the MTF, thanks to the implementation of optimised photodetectors (mainly photodiodes). Other useful features can be available such as micro-lenses and coloured filters. Today, several foundries are offering such specific CMOS processes and their number tends to increase as the photonics market (including the imaging business, and particularly the camera mobile phones market) increases. Even if the associated electro-optical performances depend on the selected foundry, typical figures that can be expected are dark current density around 100 pA/cm^2 at ambient temperature, peak quantum efficiency in the 60-70 % range and MTF close to its theoretical value.

In 2003, EADS-Astrium and Supaéro/CIMI carried out the design of a 1k x 1k 2D array (13 µm pitch) and of a 3k linear array (6.5 µm pitch) based on the use of a

0.35 µm CMOS process optimised for imaging applications. Fig. 6 shows the assembled reticule before launch into foundry, including these two devices. The arrays will be characterised in 2004 and it is expected that their electro-optical performances will show a breakthrough when compared to the ones obtained using standard CMOS technology.

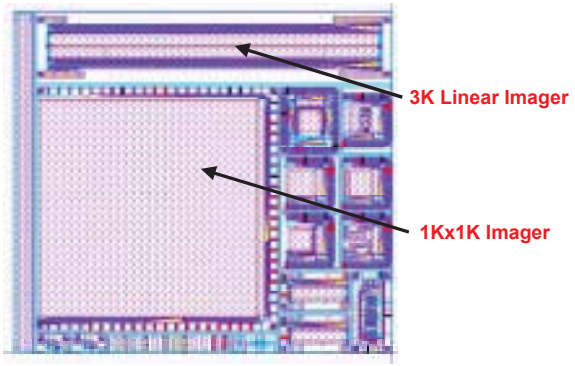

Fig. 6: assembled reticule designed by EADS-Astrium and Supaéro-CIMI before launch into 0.35 µm foundry optimised for imaging applications: the two larger devices consist of a 1k x 1k 2D array (13 m pitch) and a 3k linear array (6.5 µm pitch)

Some of the major monolithic CIS performances can even more be improved by using pinned photodiode (see Fig. 7). This type of diode, also used in interline CCDs, offers a simple way to cancel the kTC noise via a four transistors intra-pixel circuitry and to adjust the conversion factor independently of the photodiode design (see [9]). In addition, pinned photodiodes offer a reduced dark current due to the pinning of surface-interface traps, an improved blue response and a very low lag. Few large foundries over the World offer pinned photodiodes through their CMOS process optimised for CIS. It is difficult to bet that the four transistor pixel will replace the widely used 3T pixels soon as the standard pixel architecture. Indeed, the realization of such a structure presents several manufacturing challenges and might be too expensive for medium-size foundries.

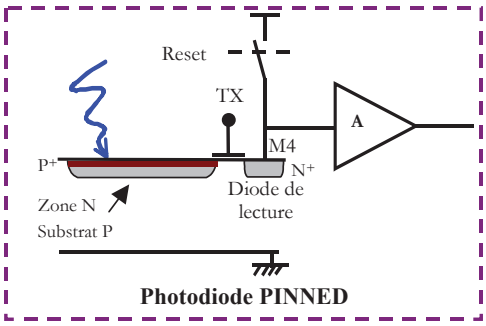

Fig. 7: synoptics of a 4 transistors pixel based on a pinned photodiode

3.3 Hybrid approach

The third way that is considered for CIS performances improvements is the hybrid approach. The idea is the same as the one used for modern cooled IR focal plane manufacturing, but exotic material (such as MCT, InSb...) is replaced by a silicon detector array. The main advantage of this approach is that it allows the independent optimisation of the photodetection layer on the one hand and of the read-out circuit layer on the other hand. In addition, hybridisation approach permits to reach 100% fill factor for the photodetector and gives more area for the associated in-pixel circuitry.

Today, manufacturers are investigating two different approaches. The first one (see [10]) consists of the use of silicon monocrystalline detection layer hybridised on top of a CMOS read-out circuit, using indium bump or loophole techniques. The two main drawbacks linked to this approach are the minimum pitch, fixed by the limitation of hybridisation (typically 10-15 µm), and the cost of the detection layer manufacturing and hybridisation processes. At least two US manufacturers are today offering such visible hybrid arrays, relying upon their IR focal planes background. A first development started in Europe in 2003 trough an ESA contract and a second development might start during 2004.

The second approach (see [11]) is based on the deposition of amorphous silicon (a-Si:H) thin film on

top of the read-out circuit. When compared to silicon monocrystalline device, this approach avoids the need for a hybridisation technique, lowering the cost and allowing small pixel pitch manufacturing. Amorphous silicon detectors are expected to offer high quantum efficiency, low dark current and excellent MTF (due to its low lateral diffusion rate). On the other hand, the spectral response of standard a-Si:H rapidly falls down over 700 nm. In addition, some electro-optical parameters are expected to be worse than for monocrystalline silicon, such as technological noise, cosmetics and lag. Today, several institutes and manufacturers are working on this promising approach.

4 CONCLUSIONS

Using standard CMOS processes, 3T photodiodes and 4T photogates CIS are today able to reach performances equivalent to standard front illuminated CCDs. At least three ways are identified to even more improve CIS electro-optical performances: (i) optimisation of the intra-pixel circuitry; (ii) use of CMOS technologies improved for imaging applications; (iii) the hybrid approach. EADS-Astrium and Supaéro-CIMI are today investigating the first two ways and should start soon tasks about the third one in order to be able to provide CMOS arrays dedicated to space applications with performances comparable to those of scientific CCDs, while keeping the advantages of CIS which can lead to dramatic space system improvements.

ACKNOWLEDGMENTS

The authors wish to acknowledge CNES and DGA for their support to the CMOS optical sensor activities for space applications. They also wish to thanks their colleagues at Supaéro-CIMI laboratory and at EADS Astrium detection laboratory, and particularly Olivier Donnadieu, Nicolas Guardiola, Céline Engel and Magali Estribeau.

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