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El-Hang Lee
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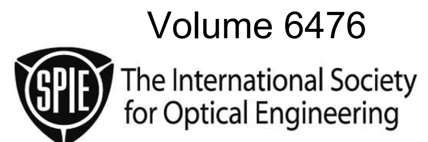

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Introduction

This volume features contributions from scientists and engineers in the general area of optoelectronic integrated circuits (OEICs). The joint session between the OEIC Conference and the Photonics Packaging, Integration, and Interconnects Conference this year resulted in valuable contributions in the areas of OEIC packaging and board-level interconnects.

Optical, electronic, and biological devices are integrated to address the issues of cost, space, performance, and reliability. Demands for greater bandwidths have driven the telecom and datacom research communities to realize complex OEICs such as transceivers, low chirp optical sources, switching systems, and multi-channel optical distribution systems. The integration of multi-wavelength laser arrays, monitoring photodiodes, and drivers is becoming a reality in the communications arena. Other emerging OEIC application areas include neural systems, optical computing, optical storage, smart pixel arrays, projection displays, imaging, scanning, printing, medical diagnosis, and chemical/biological sensing.

The increased level of integration in recent years has resulted in an increased level of miniaturization. The scientific and technological issues and challenges concerning the micro/nano/quantum-scale integration of optoelectronic devices, circuits, components, modules, subsystems and systems include the size effect, proximity effect, energy confinement effect, microcavity effect, single photon effect, optical interference effect, high field effect, nonlinear effect, noise effect, quantum optical effect, and chaotic noise effects. Optical alignment between miniature devices, minimizing interconnection and coupling losses, and maintaining the stability of optical interfaces, are some of the important issues that are receiving careful consideration.

Papers in these proceedings include discussions of the physics, theory, design, modeling, simulation, and scaling of a wide range of OEICs with regard to their optical, electrical, thermal, and mechanical properties; the integration of different optoelectronic structure types including dots, wells, planar, free space, one-dimensional, two-dimensional, and three-dimensional photonics crystals; the integration of different functions including lasers, amplifiers, detectors, sensors, modulators, isolators, circulators, switches, attenuators, couplers, multi/demultiplexers, filters, wavelength converters, polarization controllers, chromatic/polarization mode dispersion compensators, intra-chip/chip-to-board/board-level optical interconnects, and control electronics; the fabrication, processing, and manufacturing techniques (UV/deep UV/X-ray/e-beam lithography, casting, molding, embossing, etching, passivation, etc.), as well as the packaging, assembly, reliability, and qualification of monolithic and hybrid OEICs in a variety of materials (semiconductors, silica, polymers, ferroelectrics,

magnetics, metals, biomaterials, etc.). Some papers describe the refinement of existing schemes and processes, while others introduce novel concepts and new designs. Papers from academic and research institutions push the state of the art in miniaturization, level of integration, and performance figures of merit, and papers from the industry emphasize design criteria and manufacturing methods that result in practical OEICs that can be deployed commercially today or in the near future.

Although this volume cannot include all the recent important work in the vast field of OEICs, it does cover a significant cross-section of the advances happening globally in areas where OEICs are making an impact, and it provides a roadmap to the future of OEICs by presenting the cutting-edge work and the visions of leading experts who are actively inventing the future.

Louay Eldada
El-Hang Lee

Invited Paper

Flexible Polymer Pillars for Optical Chip Assembly: Materials, Structures, and Characterization

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Abstract:

In an effort to address the need for robust optical chip I/O interconnects, we describe the fabrication and testing of microscopic polymer pillars for use as a flexible optical bridge between the chip and the substrate. The polymer pillars are photoimaged using the polymer Avatrel to a height of up to 350 μm. The photodefinable polymer Avatrel was used for the fabrication of the optical pillars due to its ease of processing and its unique material properties that include high T_g and low modulus. To evaluate the performance of the polymer pillars, the optical coupling efficiency from a light source to an optical aperture with and without an optical pillar is measured. For a light source with 12º beam divergence, a 30×150 μm polymer pillar improves the coupling efficiency by 3 to 4.5 dB compared to pillar-free (free-space) optical coupling. Due to the high mechanical compliance of the optical pillars, we also demonstrate that polymer pillars enhance the optical coupling efficiency between the chip and the substrate when they are misaligned in the lateral direction and that the displacement tolerance can be doubled from 15 to 30 μm for a 1dB power loss budget.

I. Introduction

The lack of low-latency, high-bandwidth, and high-density input/output (I/O) and off-chip interconnects is a critical limiter to the performance of a gigascale system [1-3]. There are a number of challenges to achieving such interconnections using electrical interconnects, which include high losses in the substrate dielectric, reflections and impedance discontinuities, and susceptibility to cross-talk. Microphotonics technology provides an opportunity to overcome these challenges and thus, the motivation for the use of optical chip-to-chip interconnects has been presented [1-3].

Optical interconnects can be classified as either free space or guided wave. Free-space optical interconnects have been widely pursued for chip-to-chip communication [4, 5]. However, susceptibility to misalignment and complexity in packaging are formidable challenges yet to be fully addressed. Guided-wave optical interconnects using polymer waveguides, which are batch fabricated on the substrate, are also being pursued as a competing solution to how one may implement an optical chip-to-chip interconnect network [6-12]. Polymer-based optical waveguides offer a number of advantages that include high density, optical confinement, and ease of fabrication. Figure 1 illustrates two methods of achieving surface-normal optical interconnection between the chip and the substrate using planar optical waveguides. In both cases, mirror-terminated waveguides are positioned directly beneath the chip-level optical sources and

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photodetectors (PDs). In the first case (Figure 1(a)), optical interconnection is achieved through *free-space I/O* transmission. The use of microlenses to focus the light has been proposed to control beam divergence, although it adds fabrication complexity [8]. The free-space optical I/O transmission shown in Figure 1 (a) places significant constraints on the 3D spatial positioning of the optical elements relative to each other making it highly susceptible to lateral alignment deviations caused either during assembly or thermal cycling. Such misalignments could severely reduce the optical power delivered to the PD thereby increasing the bit error rate (BER) and reducing bandwidth [13].

The use of "surface-normal optical waveguides," or polymer pillars, was previously described as a means of addressing the shortcomings of free-space optical I/O interconnections [14-17]. Figure 1(b) illustrates how the polymer pillars provide optical interconnection between the chip and the substrate. The polymer pillars are designed to be mechanically compliant (flexible). The low elastic modulus of the polymer and air cladding of the waveguide contribute to the flexible nature of the polymer pillars. As a result, the lateral misalignment induced by chip-substrate CTE mismatch is compensated by the mechanical compliance of the optical pillars.

In this paper, we describe the material properties, fabrication, and optical characterization of the optical pillars. To this end, the paper is organized as follows. First, in Section II, we begin by describing the material properties of the polymer that is used to fabricate the polymer pillars. The fabrication of the polymer pillars is described in Section III. Section IV, which is an extension of [18], describes the experimental test setups used to characterize the optical performance of the optical pillars and their corresponding results. Finally, Section V is the conclusion.

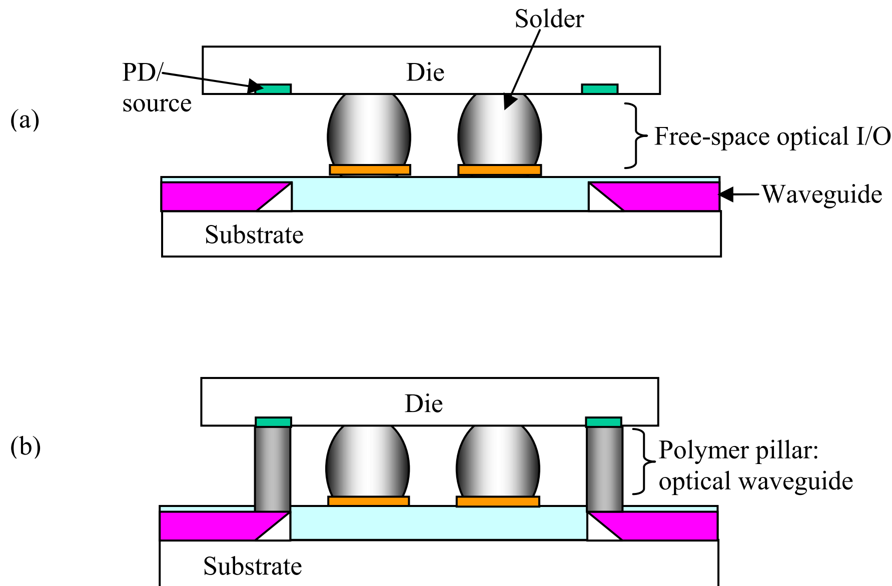

Figure 1: Schematic illustration of electrical and optical chip I/O interconnections. (a) Optical I/O interconnections are achieved using free-space transmission. (b) An optical bridge (polymer pillar) is used to optically interconnect the chip and the substrate.

II. Polymer Material Property

The Avatrel polymer is composed of addition polymerized norbornene monomer units (see Figure 2) which produces a high glass transition temperature (T_g) polymer with desirable dielectric, mechanical and optical properties (see Figure 3) [19]. The Avatrel 2580P formulation is a negative-acting photoresist composition that is sensitive to I-line (365nm) irradiation. The latent reactivity required for photodefinition is provided by epoxy moieties pendant to the polynorbornene backbone. The amorphous nature of Avatrel results in >96% transmission of near radiation UV and

visible spectrum, allowing extremely thick films (200-500 μm) to be readily photo-patterned with only moderate energy doses.

Avatrel is applied to substrates by spin coating. The high molecular weight of the polymer permits the preparation of films as thick as 100 microns in a single step. Due to the hydrocarbon nature of the polynorbornene backbone, lithiographic pattern development requires the use of an organic solvent developer.

Avatrel is a soft, elastic material, even in the final crosslinked form. Data presented below will show that the low modulus (0.45 GPa) of Avatrel permits the polymer pillars to flex under an external stress. The elongation to break of ~20% provides sufficient latitude to allow the necessary motion without inducing permanent plastic deformation of the pillar structures.

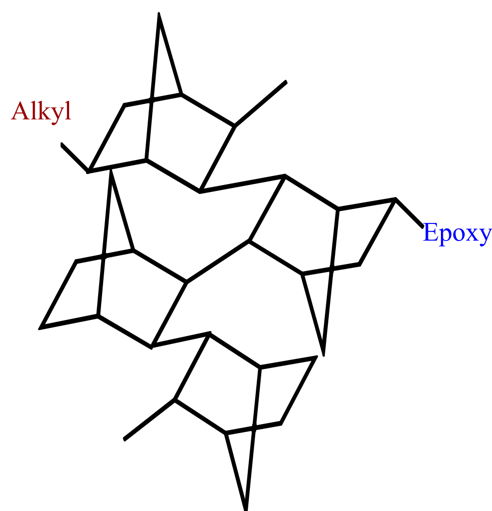

Figure 2: Polymer structure of Avatrel.

Property	Condition	unit	Avatrel 2190P
Transparency	400-700nm	% T	>96%
Refractive Index	589nm (Na D line)	-	1.537
Tensile Strength	RT	MPa	14
Tensile Modulus	RT	GPa	0.45
Elongation	RT	%	21
Dielectric Constant	1MHz/ RT	---	2.55
Dissipation Factor	1MHz/ RT	---	0.010
Volume Resistivity	RT	ohm•cm	2×10^{15}
Dielectric Strength	RT	kV/mm	296
5% Weight Loss	5C/ min	°C	291
Thermal Decomposition	5C/ min	°C	413
CTE	50 ~ 100C	ppm	197
Tg	5C/ min	°C	220
Water Absorption	24hr/ RT	%	0.14
Adhesion to SiN	PCT	Pieces*	0/100
Adhesion to SiO2	PCT	Pieces *	0/100

Figure 3: Material properties of the polymer Avatrel.

III. Polymer Pillar Fabrication

The process that is used to fabricate the polymer pillars on a substrate containing optical devices is shown in Figure 4. The fabrication process begins by spin coating the polymer Avatrel to a thickness equal to the desired height of the polymer pillars. The substrate is next placed on a hotplate (100°C) to soft bake the polymer. Next, the polymer film is UV irradiated (365 nm) through a mask containing the cross-sectional geometry of the polymer pillars. Following UV irradiation of the polymer film, the glass wafer is placed in a nitrogen purged oven (100°C) for a hard bake. Next, the polymer film is spray developed using Avatrel Developer to yield the polymer pillars. Finally, the wafer is placed in a nitrogen-purged oven where the polymer is cured at a temperature of 160°C for 1-hour. SEM images of polymer pillars with various dimensions are shown in Figure 5.

In this study, the polymer pillars were fabricated above open metal apertures on a transparent (glass) substrate. Such a configuration enables us to attain optical access to both ends of each polymer pillar, which is needed for its optical characterization. The fabrication process that was used to fabricate this configuration is shown in Figure 6. A metal film is first deposited and patterned on a glass substrate (Figure 6(b)). In this case, a 600 nm thick layer of aluminum was used. The diameter of the circular optical apertures through the aluminum was fabricated to be equal to the diameter of the polymer pillars. Next, silicon dioxide was deposited above the patterned metal film to enhance the adhesion of the polymer pillars to the substrate. The polymer film is next spin coated and soft baked (Figure 6(c)). By mounting the substrate upside down in a mask aligner, the same optical apertures that would be used for optical testing were used as a mask to photopattern the polymer film with the cross-sectional geometry of the pillars (Figure 6(d)). Following exposure, the fabrication steps outlined previously (above) are implemented. Using this fabrication process, 30 μm diameter and 150 μm tall (30x150 μm) and 50x150 μm polymer pillars were fabricated.

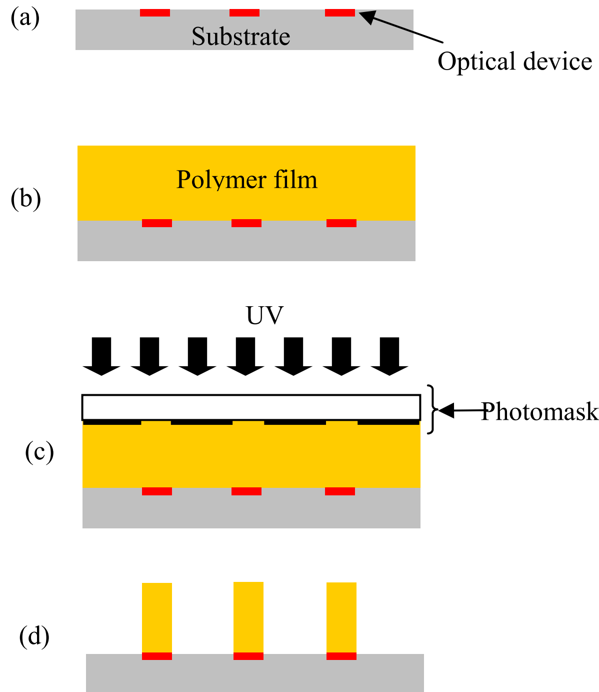

Figure 4: Schematic illustration of the process used to fabricate optical polymer pillars directly above optical devices.

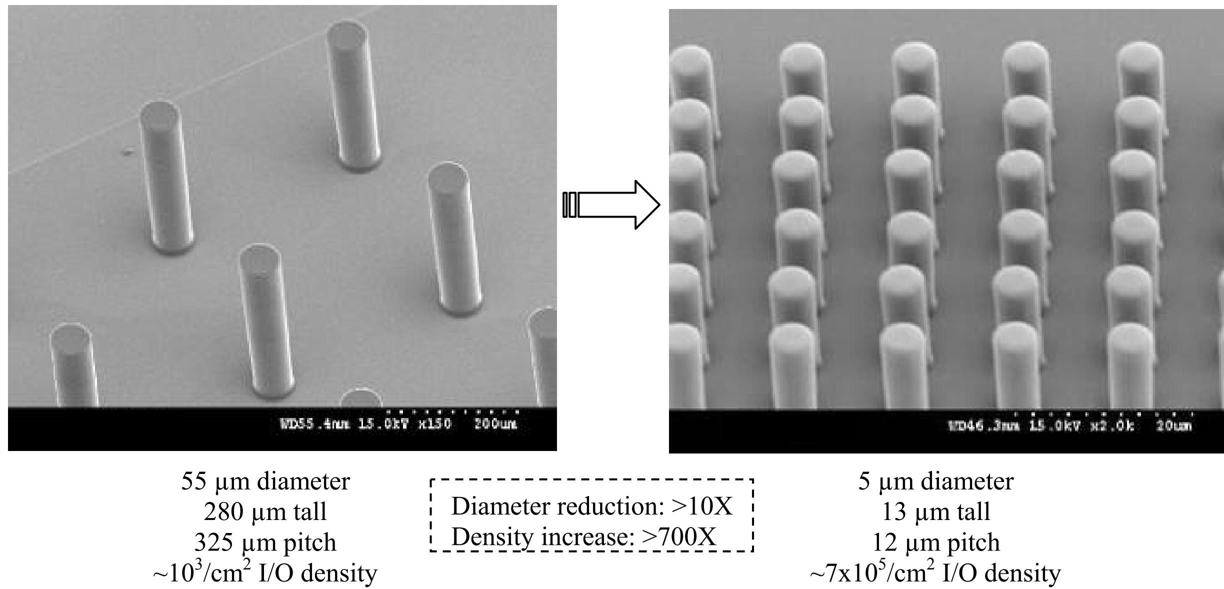

Figure 5: SEM images of polymer pillars with various dimensions and pitch.

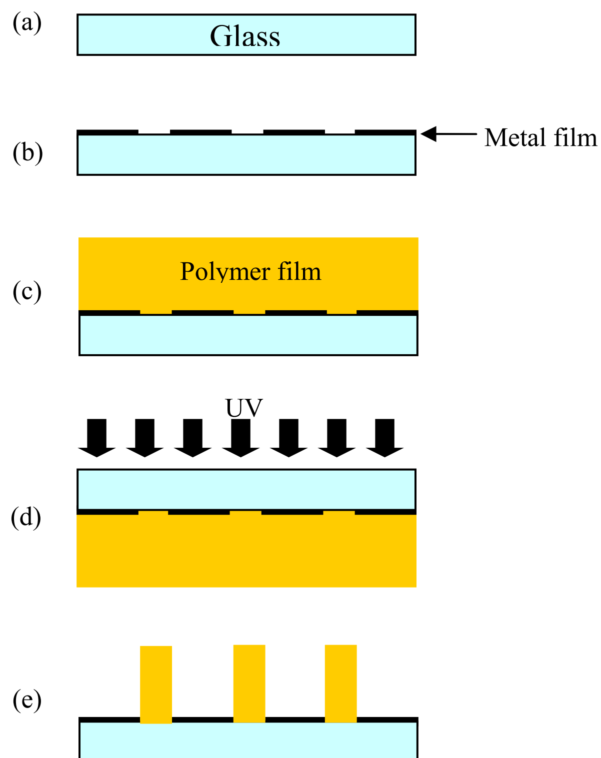

Figure 6: Schematic illustration of the process used to fabricate polymer pillars in this study.

IV. Optical Testing

Using the experimental setup shown in Figure 7, the optical coupling efficiency between a light source and an optical aperture with and without a polymer pillar was measured. This measurement setup provides insight into how the optical coupling efficiency differs between the two optical I/O schemes shown in Figure 1 (free-space transmission vs. optical (pillar) bridge). A multimode fiber with 12° divergence angle was used as the light source. For each case, the transmitted optical power was measured with a Si detector as a function of the fiber (light source) position in the lateral direction.

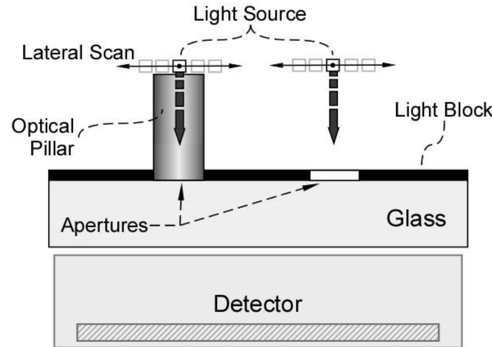

Figure 7: Experimental setup used to characterize the optical coupling efficiency improvement due to the use of a polymer pillar between a light source and an optical aperture.

In this measurement, the optical aperture was 30 μm in diameter and the polymer pillar was 30 x 150 μm. The distance between the surface of the metal film and the fiber was kept constant and at a distance equal to the pillar's height (150 μm). The fiber was scanned in the X-axis and in the Y-axis above the end-face of the pillar and above the aperture. The relative transmitted optical intensity for both sets of measurements is plotted in Figure 8 (a). The transmitted intensities are normalized to the maximum transmission at the center of the open aperture without a pillar. The X- and Y-axis scans are essentially equal due to the radial symmetry of the light source and the pillars. The difference between the coupling efficiency of the two measurements (using data from the X-axis scan) is plotted in Figure 8 (b). The data clearly demonstrate that at the 0 μm displacement position, the polymer pillars enhance the optical coupling efficiency by approximately 3 dB when compared to direct coupling into the aperture. The polymer pillar improves the coupling efficiency by 4.5 dB at the edges. The coupling improvement is significantly larger than the 0.2 dB excess loss of the pillars [18] thereby clearly demonstrating their benefits. This improvement in the coupling efficiency could easily result in the BER improvement by many orders of magnitude. Note that the profile of the relative intensity curve of the polymer pillar is almost flat across the entire end-face of the pillar and abruptly drops beyond the edges of the pillar (X=±15 μm). On the other hand, the intensity curve of the aperture resembles an inverse parabola. This is important because it signifies the importance of having perfect alignment for the direct coupling case shown in Figure 1(a). Any misalignment in the lateral direction would cause a fast roll-off in the transmitted intensity. Even with perfect alignment during assembly, any lateral misalignment between the mirror and the detector due to either CTE mismatch or other factors would reduce the coupling efficiency and limit the achievable bandwidth.

The experimental setup used to characterize the lateral displacement optical compensation of the polymer pillars is shown in Figure 9. In this measurement, a 50x150 μm polymer pillar was used. To quantify the effects of pillar bending on optical signal transmission, two experimental configurations, shown in Figure 9, were developed. In the first configuration, which is labeled "scanning" in the figure, the light source (fiber) is scanned laterally across the end-face of the pillar (similar to earlier measurement). In the second configuration, which is labeled "pillar bending" in the figure, the fiber is attached to the end-face of the pillar using epoxy to form an air-free light pass between the source and the substrate. In the "pillar bending" case, the controlled lateral displacement of the light source causes the polymer pillar to bend sideways helping to keep the lightmode confined in the pillar and thus, to deliver the optical signal to the detector with lower coupling losses.

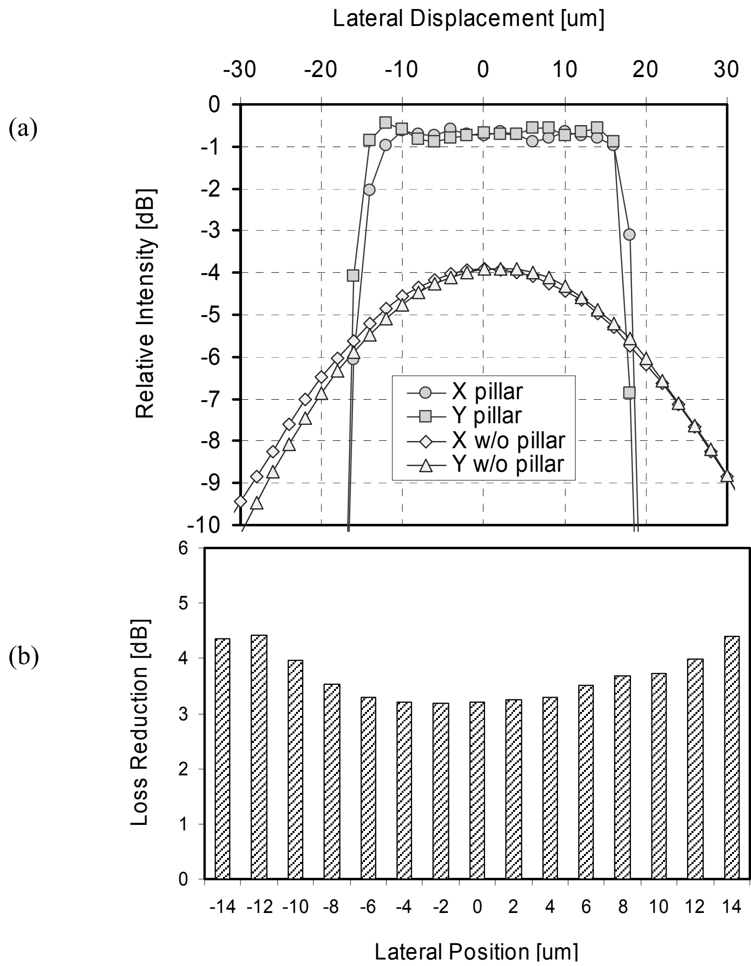

Figure 8: (a) Lateral intensity scans for coupling improvement measurements. (b) Coupling loss reduction (due to optical pillar) as a function of lateral position of the light source.

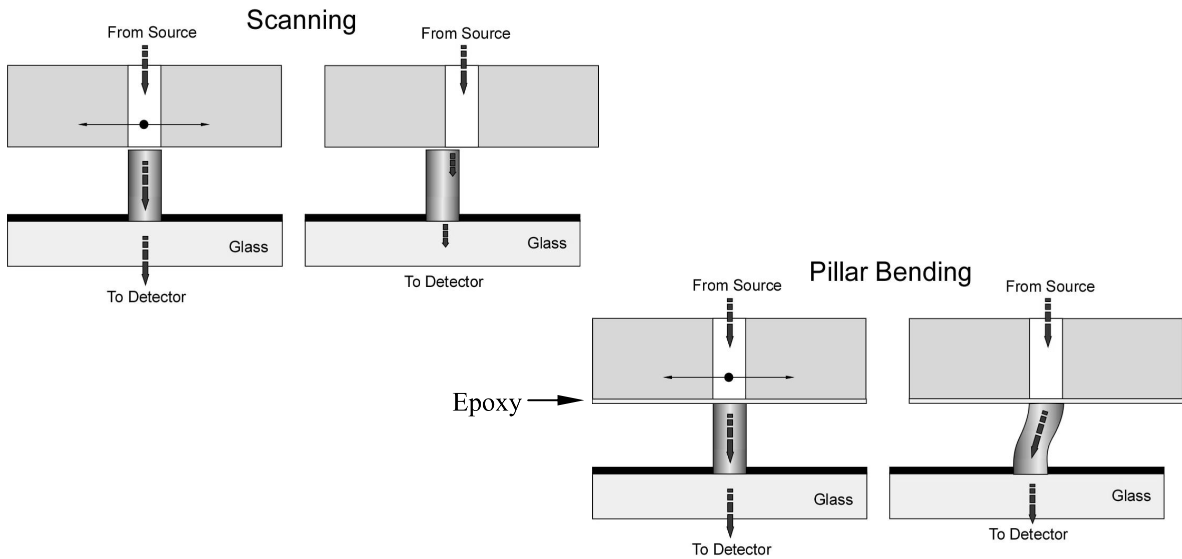

Figure 9: Schematics of the experimental setups used to evaluate the optical displacement compensation of the polymer pillars.

The relative transmitted intensities as a function of lateral displacement of the light source for the two experimental configurations illustrated in Figure 9 are shown in Figure 10. As can be seen from Figure 10 (a), the use of the refractive index matching epoxy to glue the fiber to the end-face of the pillar decreased the optical losses at zero displacement by 0.2 to 0.3 dB. Thus, by simply eliminating the air-gap between the pillar and the optical source, one automatically gains a reduction in the coupling loss because the air-free pass minimizes the Fresnel back-reflections. Figure 10 (b) shows the loss reduction due to the use of pillar bending at different light source displacements. The loss reduction is less than 1 dB up to 15 μm displacement and increases up to 4 dB at 30 μm. Since optical power loss has a critical effect on the BER of a digital system, minimizing losses is very important. Therefore, usually only a limited loss budget is available in the system for misalignments to maintain the error-free operation. Figure 10(a) undoubtedly demonstrates that for a given loss budget of, e. g., 1 dB, the 50×150 μm flexible pillar doubles the displacement tolerance from less than 15 to about 30 μm. The 4 dB pillar-assisted loss reduction at the 30 μm displacement can easily decrease the BER by 10^4 or more. Thus, the polymer pillars provide a method of reducing optical coupling losses caused by thermo-mechanically induced optical misalignment between the CTE mismatched chip and substrate.

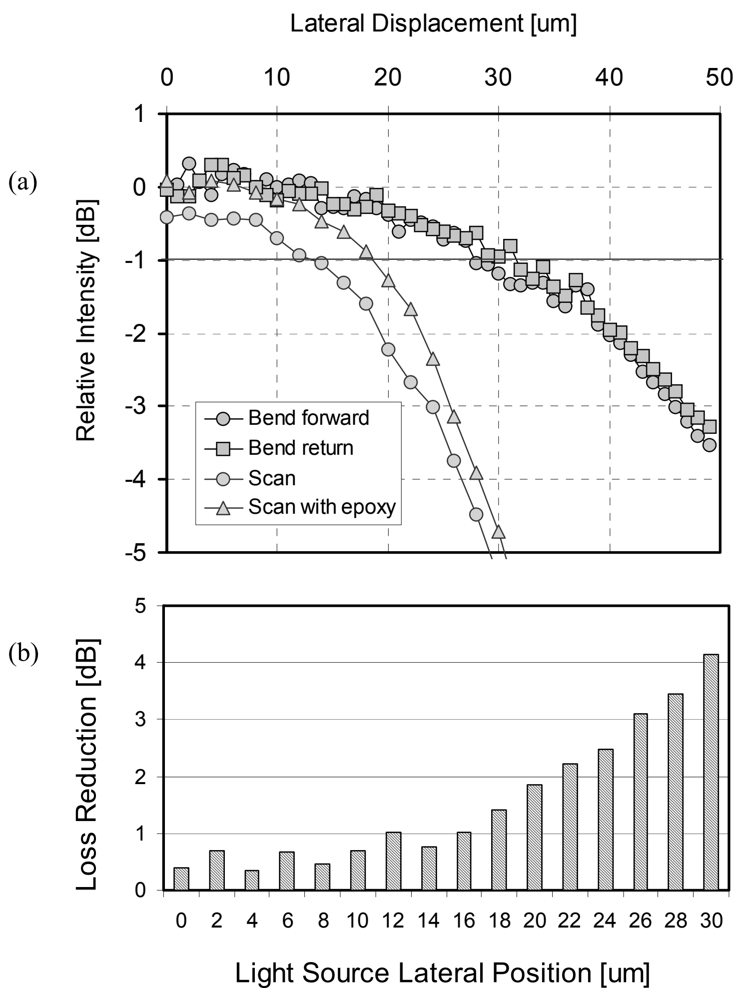

Figure 10: Optical displacement compensation with flexible pillars.

V. Conclusion

The use of polymer pillars to enhance surface-normal optical coupling efficiency between chip-level optical devices and substrate-level waveguides is experimentally demonstrated. The photodefinable polymer Avatrel was used for the fabrication of the optical pillars due to its ease of processing and its unique material properties (high T_g and low modulus). Using 30 μm diameter apertures and 30x150 μm optical pillars, the improvement in the coupling efficiency due to the polymer pillar was 3 to 4.5 dB, which would ultimately improve the BER of a digital system by orders of magnitude. Moreover, the mechanical compliance of the polymer pillars significantly improves the displacement tolerance of the assembled parts, which is especially important due to the CTE mismatch between the chip and the substrate. The displacement tolerance was doubled from 15 to 30 μm in the case of a 50×150 μm pillar for a 1dB power loss budget. It is expected that polymer pillars with larger aspect ratios and smaller diameters can provide even higher displacement compensation in dense chip-to-chip optical interconnect modules.

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Optoelectronic Packaging for 16-Channel Optical Backplane Bus with VHOEs

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Abstract

A novel 16-channel optical backplane bus with volume holographic optical elements (VHOEs), operating as diffraction grating beam alignment guides, was designed and fabricated for a high-performance computing system multi-slot bus. These thin film VHOEs were fabricated to diffract light beams for each bus slot into a glass wave-guiding plate (refractive index 1.52) for total internal reflection to other slot positions. Slot-to-slot optical alignment issues, including channel crosstalk and beam alignment tolerances, were computer modeled to optimize a low cost and simple optical packaging structure. For each slot position, a 4 X 8 element optical packaging plate was then fabricated to allow insertion of 16 VCSELs and 16 Photodiodes, each in an individual TO-46 can.

Through the VHOE, the slot-to-slot fan-out received beam intensities were experimentally measured for each of the 16 channels and found to be in the range of 90 μW ~ 150 μW. This 90 μW minimum fan-out power is 5dB greater than the receiver sensitivity requirement. In this study, the maximum 10 Gbps single channel bandwidth was tested and a 1.6 Gbps aggregate bandwidth was also demonstrated through a three slot 16-channel optical backplane bus. This aggregate bandwidth was limited by an electronic element in the receiver circuit (155 Mbps PD-TIA) and processor (100 Mbps FPGA). With the system's measured optical isolation of greater than 80dB, and suitably fast receiver electronics, simulation modeling indicates that Terabit per second bus data rates can be achieved in inexpensive, mechanically robust and reliable form factors.

Index Term – Optical Backplane Bus, Volume Holographic Optical Elements (VHOEs), VCSEL, Photodiode, Lateral and Angular Misalignment, Optical Packaging Plate.

1.Introduction

Due to the rapid and wide expansion of the internet service, every personal computer is now connected to every other computer all over the world. The number of computers and servers connected with the internet has increased every year. The amount of data also increased because large amounts of data can be handled by the increased execution speed of the central process unit (CPU). The most recent International Technology Roadmap for Semiconductors (ITRS) projects that while per-chip performance will continue to improve at a rate of approximately four times every three to four years, the number of signal pins per module will only double over the same period, and the maximum bit rate per signal pin will increase by only 35% [1]. By 2010, the requirement for off-chip

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clock frequency will reach more than 12 GHz. Also, modern multiprocessor computer architectures place stringent demands on the inter processor connection schemes. Thus, the total off-chip I/O bandwidth, pin count times bit rate per pin, will increase by roughly 2.7 times, while the internal chip performance improves by four times [2] per process cycle.

An unfortunate consequence of this improvement rate mismatch is that system computing performance is not proportional to the increase in number of processors. In a typical system, processors and memory are distributed across several different nodes, and data must be constantly transferred between them as computing operations occur. The performance of multiprocessing systems is mainly limited by the bandwidth, the power consumption and delay of electrical interconnections. Electrical interconnects cannot achieve sufficiently high data rates using traditional bus architecture, so utilizing large numbers of point-to-point interconnects has become a popular choice for high speed system. Therefore, wiring congestion is a concern for high performance computing. A 10Gbps high-speed electrical backplane using point-to-point link has been demonstrated by Sinsky *et al.* [3]. A bit error rate (BER) of less than 10^{-13} was achieved over an 87 cm transmission line using duobinary signal encoding. Recently, data transmission at 25 Gbps over a 61 cm link (15.25 Gbps·m) on an electrical backplane was demonstrated by the same group [4]. Electrical backplane can support, in theory, 100 Gbps Ethernet applications using conventional backplane design techniques (four channels at 25 Gbps). However, a detrimental drawback of the approach is the high signal loss over the link of −50 dB at 25 GHz due to skin effects and dielectric losses in the FR4 material [5].

On the other hand, optical backplanes permits different daughter boards to share the transmission channel while maintaining extremely high data rate, and therefore does not have wiring congestion problem. We demonstrated the first optical backplane bus with the volume holographic gratings at 15 Gbps data rate per channel [6,7]. In such an optical backplane, a bus architecture is retained to fulfill the task of broadcasting and transmission channel sharing, while the potential data rate is comparative to or even higher than that in electrical point-to-point type backplane, as long as high-speed electro-optical transceivers are available. The optical backplane bus uses optical signal to realize communications for board-to-board interconnection. Each board is equipped with optoelectronic transceivers (VCSELs and photodiodes) for the emission and detection of modulated optical signals. Several optical bus architectures based on the optical backplane have been proposed including the substrate-mode guided-wave bus system implemented with wave-guiding plates and holographic grating elements [7,8,9,10] and the free-space bus systems implemented through free-space optical interconnections [11,12].

In this paper, a novel 16-channel optical backplane bus with VHOEs was fabricated and successfully demonstrated with a computing system involving processor and memory modules. As shown in Fig. 1, the optical backplane bus contains TO-46-CAN packaged 1.5 Gbps VCSELs and 622Mbps photodiodes (with 155 Mbps TIA) as an optical transmitter and receiver, respectively. The volume holographic grating films are recorded to diffract light beams (λ = 850 nm) into a glass wave-guiding plate (refractive index 1.52) for total internal refraction. To reduce packaging difficulties, a novel 4 X 8 optical packaging plate is designed for 16-channel optical backplane bus system. Packaging issues including crosstalk and alignment tolerance were theoretically studied to design optical packaging

structure. Although each individual channel shows the maximum bandwidth of 10 Gbps, the system demonstration reported herein is limited by the processor (Xilinx FPGA, Virtex4-FX60) which has 100 Mbps channel data rate.

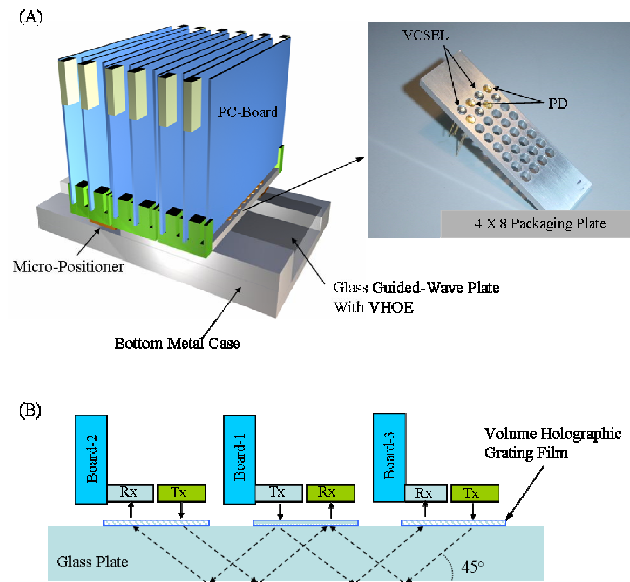


Figure 1 (A) Schematic 3-D view of 16-channel optical backplane bus with the volume holographic gratings. A 4 X 8 optical packaging plate for packaging of optoelectronic devices (16 VCSELs and 16 Photodiodes are packaged alternatively). (B) Schematic view of optical signal redirection mechanism by the volume holographic gratings and a glass guided-wave plate. (▩ : double grating hologram, ▨ **:** single grating hologram)

II. Fabrication of Volume Holographic Grating Films and Optical Packaging Plates

The photopolymer-based volume hologram is an attractive option for making high-efficiency gratings. A single hologram grating is recorded in DuPont photopolymer (HRF-600) film to precisely redirect input/output signal beams at 45° zigzag bouncing angle. The thickness of the photopolymer film is 10 μm. The Verdi laser (λ = 532 nm) is used for recording photopolymers. The photopolymer emulsion is insensitive at 850 nm, which allows *in-situ* monitoring at this wavelength. The diffracted light from an 850 nm probe laser was monitored to measure the dynamic diffraction efficiency.

There are 4 pieces of the volume holographic films on the glass substrate. *In-situ* monitored hologram efficiencies, during the recording process [13], are 54.9%, 45.4%, 68.4% and 42.5%, respectively. The size of the hologram film on the center and the sides (A and B) are 50 X 30 mm^2 and 50 X 40 mm^2, respectively. To reduce the output beam diverge angle of VCSEL and to converge the input beam of photodiode, an individual dome-lens installed TO-46-CAN packaged VCSEL and photodiodes are used in this study.

Due to the optical crosstalk between the adjacent optical bus lines, the minimum pitch between two adjacent photodiodes must be determined according to the requirement

of the optical signal-to-noise (SNR) ratio. Since commercial TO-46-CAN packaged VCSEL and photodiode have the same physical radius, the minimum pitch in 4 X 8 row-and-column pattern packaging is 4.77 mm.

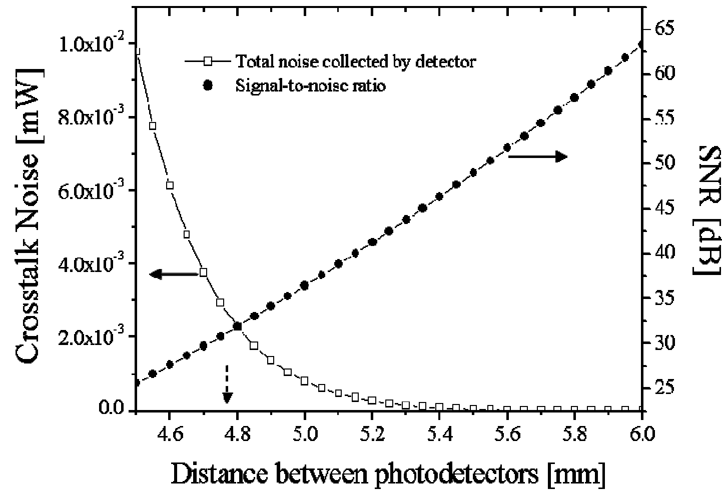


Figure 2 Calculated crosstalk and optical signal-to-noise ratio (SNR) as a function of photodiode pitch (with R = 2.38 mm) in the row-and-column pattern packaging plate.

Fig. 2 shows that the calculated signal-to-noise ratio and crosstalk noise as a function of the distance between photo-detectors [PD 622Mbps & TIA 155Mbps]. As the pitch increases above 5 mm, crosstalk noise decreases and then disappeared below 1 µW. Also the geometrical optical path-length (30 mm) through VHOE and mechanical machining tolerances (± 0.25 µm) are considered in designing 4 X 8 row-and-column pattern packaging plates. In this study, 5.5 mm pitch optical packaging plates are fabricated. The distance between photodiodes after packaging, the diagonal distance in the row-and-column pattern, is 7.78 mm. Therefore, as based on Fig. 4, the optical crosstalk noise effect, measured at greater than 80 dB cross signal rejection, can be disregarded between two detectors in this packaging plate.

The influence of angular misalignment on lateral misalignment arises from the phase mismatch between the input signal beam and the grating vector when the incident angle deviates from the Bragg angle. Fig. 3-(A) shows the phase matching conditions of a volume holographic grating for surface-normal coupling.

For the Bragg condition, the relation between the incident angle and the diffracted angle is

$$\begin{pmatrix} -\sin\gamma \\ \cos\gamma \end{pmatrix} = \begin{pmatrix} \dfrac{\sin\theta}{n} - \dfrac{K}{\beta}\sin\phi \\ \left(1 - \dfrac{\sin^2\theta}{n^2} - \dfrac{K}{\beta}\cos\phi\right)^{1/2} \end{pmatrix} \qquad (1)$$

where n is the refractive index of the hologram, $\beta(=2\pi n/\lambda)$ is the propagation constant of light with wavelength λ, and the meaning of γ, θ and K are as shown in Fig. 3-(A). After eliminating ϕ and differentiating the resulting equation, we have

$$\Delta\gamma = \frac{\left[\sin\theta - n\left(\dfrac{K^2}{2\beta^2} - 1\right)\sin\gamma\right]\cos\theta}{\left[\left(\dfrac{K^2}{2\beta^2} - 1\right)\sin\theta - n\sin\gamma\right] n\cos\gamma}\Delta\theta \qquad (2)$$

A variation of the angle of the input light beam leads to a spatial shift of the fan-out beam on the device surface of

$$\Delta L = \frac{\tan(\gamma + \Delta\gamma) - \tan\gamma}{\tan\gamma} \cdot L \qquad (3)$$

where, L is the distance between input and output beam positions.

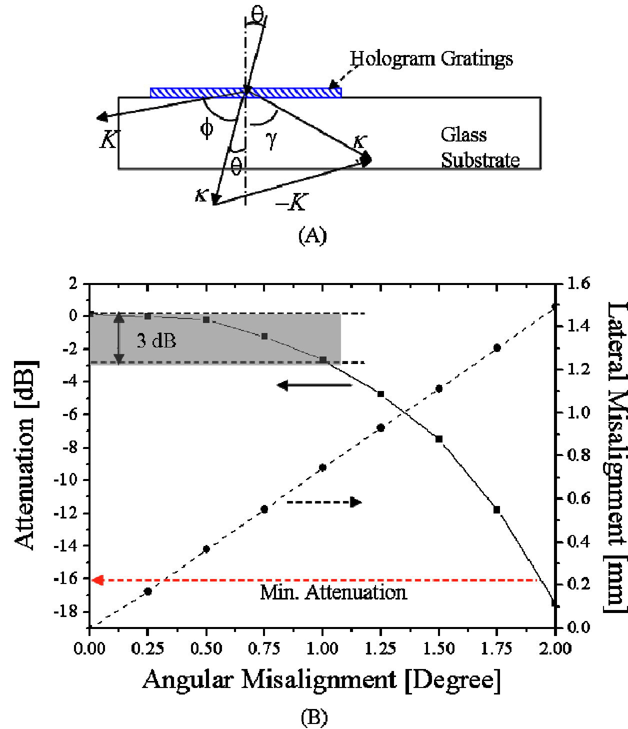


Figure 3 (A) Phase-matching diagram correlating the grating vector K, the incident beam k, and the diffracted beam k\` for a slanted holographic grating element. (B) Measured fan-out power loss and calculated lateral misalignment (*ΔL*) as a function of input beam angular misalignment (*Δθ*)

Fig. 3-(B) shows the calculated lateral deviation (ΔL) as a function of the incident angle ($\Delta\theta$) and measured fan-out power intensity variations as a function of in-put beam angular misalignment ($\Delta\theta$). Experimental results show that a 1° angular misalignment accompanied by 3dB fan-out power loss and it is related to a 0.76 mm lateral misalignment, concurrently. To obtain maximum fan-out power through VHOE, during VCSEL packaging, the angular misalignment is minimized below 1° and induced lateral misalignment can be adjusted using a micro-stage assembled with an optical packaging plate as shown in Fig. 1.

III. VCSEL Packaging to Equalize Fan-out Beam Broadcasting

To optically interconnect 4 X 8 Tx-Rx arrays using VHOEs as shown in Fig. 4, the recorded volume holographic grating films are attached on the glass substrate. The optical input signal beams, vertical to the holographic film surface, are refracted at 45° by slanted fringe structures of transmission volume holographic gratings. Due to the total internal reflection, coupled input beams are propagating through a glass wave-guiding plate and then coupled out by the matched holographic grating films.

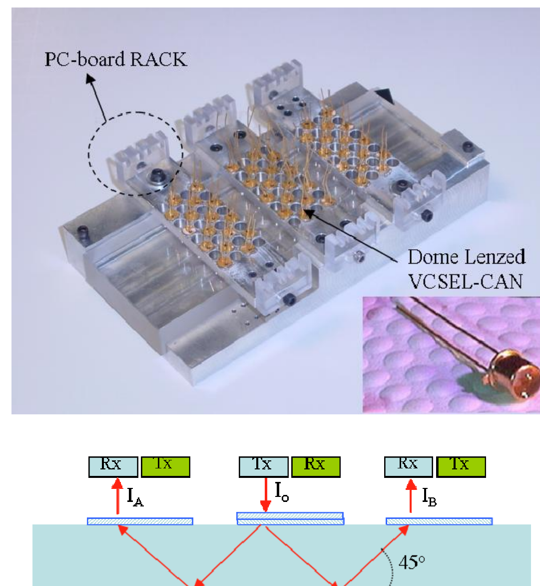


Figure 4 Assembled optical packaging components. 48-VCSELs are assembled onto 4 X 8 optical packaging plates. A glass substrate with the volume holographic gratings is assembled by a bottom metal case structure. Electrical PC-boards are assembled using rack structures. (The bottom figure shows a schematic view of equalized fan-out beam directions through the volume holographic gratings)

Fan-out beam intensity depends upon not only the diffraction efficiency of the hologram film but also the input beam incident angle as shown in Fig. 5. Therefore, the

uniformity of the fan-out beam intensity through VHOEs is one of the critical issues in this system. The measured surface area of a single hologram film, covering 4 X 8 packaging array, is 21.28 X 43.3 mm^2. A 2 mW (1.88 V / 11 mA) VCSEL beam is used as an input source (I_o). 32-point fan-out beam intensities (I_A and I_B) are measured using 4 X 8 packaging plates (4-columns and 8-rows) shown in Fig. 4. Experimentally measured 3-D fan-out beam intensity profiles are shown in Fig. 5. From the system power budget point of view, the fan-out beam intensities should be larger than the minimum value of photo-sensitivity, 20 μW, of photodiode with TIA to provide decent power margin. All fan-out beam intensity values through VHOEs are in the range of 53.2 μW ~ 165.6 μW. The average intensity values in the center and the edge of holographic grating film are 135 μW and 80 μW, respectively.

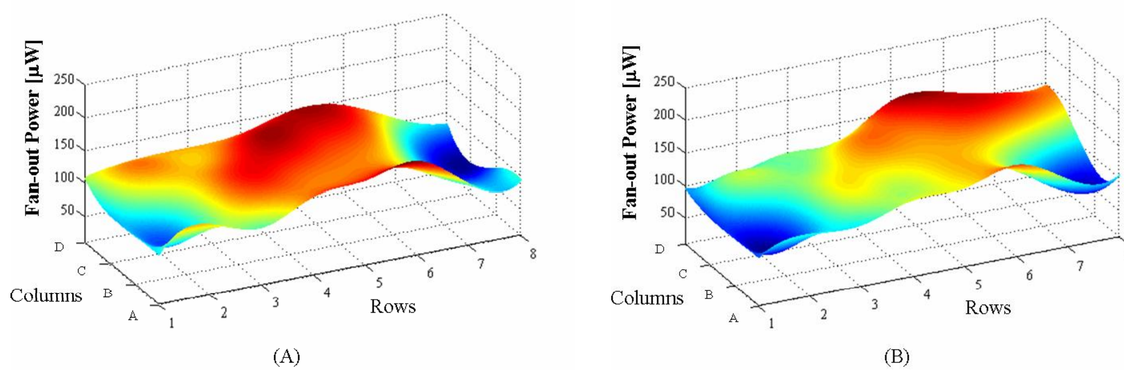
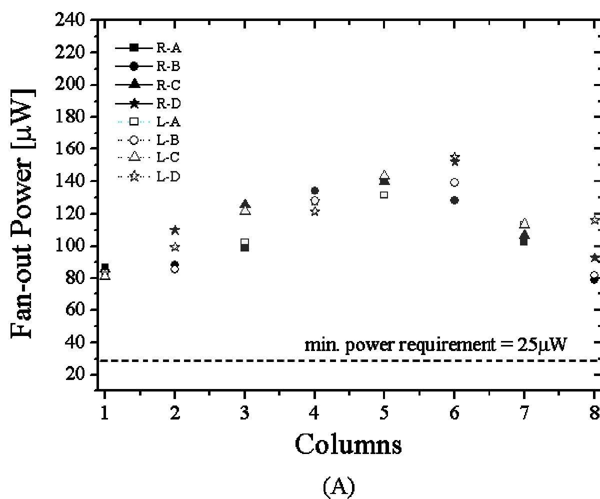


Figure 5 Measured equalized fan-out power (I_A & I_B shown in Fig.5) uniformity through volume holographic grating films.(A) Equalized fan-out power distribution through $I_o \rightarrow I_A$, (B) Equalized fan-out power distribution through $I_o \rightarrow I_B$

Since 16-VCSELs and 16-photodiodes are alternatively packaged into 32 packaging holes (4 X 8 row-and-column pattern as shown in Fig. 1), 16-channel fan-out powers from the center plate to the sides (left and right), and vise versa, are measured. During VCSEL packaging, fan-out beam intensities are simultaneously monitored and the optimum packaging position is adjusted to achieve even fan-out power through VHOEs.



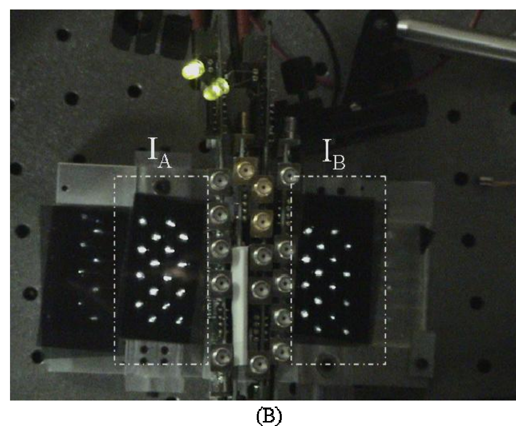


Figure 6 (A) Measured 16-channels equalized fan-out powers (I_A & I_B shown in Fig.5) through VHOEs [plate(R/L)-row, I_0 = 2 mW] (B) Far-field images of 16-channel equalized fan-out beams through VHOEs [16 beam spots inside the boxes (I_A & I_B shown in Fig.5) show the far-field images of 16 VCSEL beams diffracted by volume holographic optical elements (VHOEs)]

Fig. 6-(A) shows that 90% of 16-channel fan-out beam intensities are in the range of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system. The far-field image of 16-channel equalized fan-out beam is measured by a CCD camera as shown in Fig. 6-(B). Broadcasting 16-channel beam spots are clearly shown on the both sides of the package plate.

IV. System Assembly and Performance Test

All optical components, VCSELs, Photodiodes and VHOEs, are precisely assembled using optical packaging plates and the metal case structure shown in Fig. 4. The center packaging plate is physically bolted on the case. Two side packaging plates are designed to move laterally within a range of ±1.5 mm using micro-stage. In each optical plate, 16-VCSELs and 16-Photodiodes are arranged in row-and-column pattern as shown in Fig. 1.

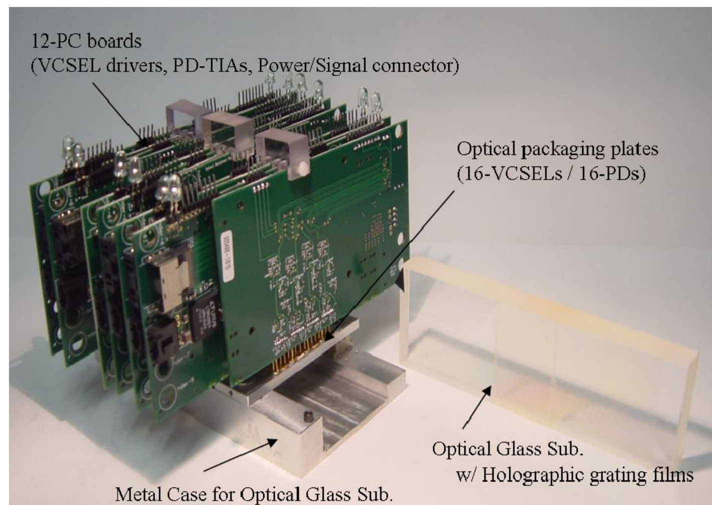


Figure 7 Assembled 16-channel optical backplane bus. PC-boards containing VCSEL drivers (3.2Gbps), PD-TIAs (155 Mbps), power/signal connector are connected with optoelectronic devices. An optical glass substrate with the volume holographic grating films

Optical guided-wave glass plate with the volume holographic grating films is also inserted into the case and then mechanically assembled. A total of 48-VCSELs and 48-PDs are precisely aligned and then packaged to get maximum fan-out power distributions. Electrical control boards are located on the top of the packaging plate as shown in Fig. 7.

Each electrical board contains 4-VCSEL drivers and 4-PD-TIAs (trans-impedance amplifiers). Four PC-boards are assembled on a single optical packaging plate to control the 16-VCSELs and 16-photodiodes. A total of 12 PC-boards are plugged to control 48-VCSELs and 48-photodetectors in this system.

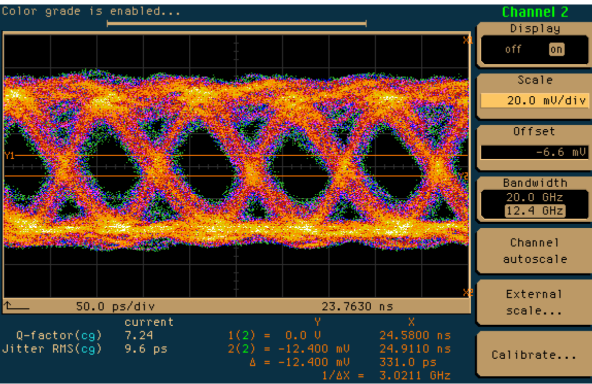
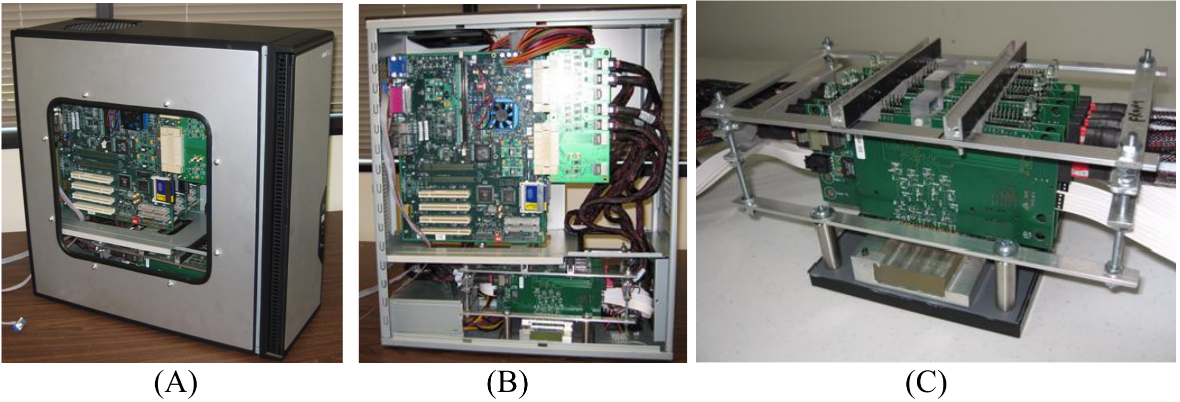


Figure 8 10 Gbps single channel eye-diagram through optical backplane bus system using Thin Film Hologram Grating.

Fig. 8 shows a single channel eye-diagram at 10 Gbps through the optical backplane measured by a digital communication analyzer (HP-83480A). The pulse pattern generator provides the modulation by generating a 2^{23}-1 pseudorandom bit sequence (PRBS) non return-to-zero (NRZ) pattern. Measured Jitter-RMS and Q-factor are 9.6ps and 7.24, respectively. Although each individual channel has the maximum bandwidth of 10 Gbps, the system demonstration reported herein is limited by the processor (Xilinx FPGA, Virtex4-FX60) which has 100 Mbps channel data rate.

All channels are individually tested and optical connection performance between VCSEL and photodiode through VHOEs is verified. All optical and electrical components are connected properly using cable connectors. The optical part (shown in Fig 7) consists of the hologram based optical backplane and 12-PC-boards containing VCSEL drivers, PD-TIAs, power connectors and signal connecters.



(A) (B) (C)

Figure 9 (A) Demonstration setup for high performance computing system with 16-channel optical backplane bus. (B) Inside view of computing system, FPGA (Xilinx Virtex-4) and memories control electrical signals through 16-channel optical backplane bus which transfer data optically. (C) Packaging set-up for Optical backplane bus.

The electrical part consists of 3 signal control boards and computing modules to operate a high speed computing system. The high speed computing system demonstration is performed using the setup shown in Fig. 9. In this demonstration, the computing system controls two FPGA boards to monitor BER (Bit Error Rate) test using 10,000 date packet per single channel. All 16 channels are monitored simultaneously. BER test result shows no error data transfer through the 16-channel optical backplane bus with VHOEs. Total 64 channels including 32 broadcasting channels are successfully demonstrated with the commercial computing system. With the system's measured optical isolation of greater than 80dB, and suitably fast receiver electronics and processor, simulation modeling indicates that Terabit per second bus data rates can be achieved in inexpensive, mechanically robust and reliable form factors.

V. Conclusions

A novel 16-channel three slot optical backplane bus is designed and fabricated using thin film volume holographic gratings to demonstrate a high-performance computing system multi-slot bus. Individual channel performs the maximum bandwidth of 10 Gbps. In this study, a 1.6 Gbps aggregate bandwidth was demonstrated through a three slot 16-channel optical backplane bus. In this demonstration, this single channel bandwidth limitation is due to an electronic element in the receiver circuit (155Mbps PD-TIA) and processor (100 Mbps Xilinx FPGA). All channels are individually tested and optical connection performance between VCSEL and photodiode through VHOEs is verified.

Thin film volume holographic gratings were fabricated to refract light beams into a glass wave-guiding plate for total internal reflection. Through the VHOEs (Volume Holographic Optical Elements), equalized fan-out beam intensities were experimentally measured. Packaging issues including crosstalk and alignment tolerance are theoretically studied to design a low cost and simple optical packaging structure. A 4 X 8 optical packaging plate is fabricated to assemble 16-VCSELs and 16-Photodiodes. VCSELs and photodiodes are inserted alternatively into 32-holes drilled with a 4 X 8 row-and-column pattern optical packaging plate. 16-channel fan-out beam intensities are in the range of 90 μW ~ 150 μW. Moreover, the measured minimum fan-out power is 78.9 μW which is 5dB higher than the minimum power requirement of this system.

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Low cost optical interconnects

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ABSTRACT

Optical interconnects to couple light from single mode fiber to waveguides and photonic elements have remained expensive due to tight alignment tolerances, materials choices, fabrication methods and assembly processing techniques. Methods that have been used to lower the cost of optical interconnects will be reviewed and compared to current and future market application demands. Design approaches, fabrication methodologies, and assembly processing techniques for optical interconnects to meet future lower cost market application demands will be shared.

Keywords: optical interconnect, low cost, fabrication methods, assembly processing

1. INTRODUCTION

Optical interconnects couple light signals to and from optical fibers, optical waveguides, and optoelectronic chips such as photodetectors and lasers. Coupling alignment requirements range in dimension from wide tolerances for multimode fiber (MMF) with core dimensions of 50 !m or 62 !m to narrow tolerances for coupling to single mode fiber (SMF), core dimension typically 9 !m.

The costs of optical interconnects and device packaging has been a determining factor in the cost for optical communication transponders as detailed in Figure 1 of reference 1. Costs for optical couplers are driven by optical alignment tolerances, application requirements, and the market size.

Cost is a relative term. For example, an optical interconnect that may be considered low cost for telecommunications applications far exceeds allowable costs for Fiber-to-the-Home (FTTH) applications. Likewise, the cost for traditional fiber connectors may exceed the total transponder cost for chip-to-chip communications applications by one order of magnitude.

2. OPTICAL COUPLING COST DRIVERS

Costs for optical interconnects include their bill-of-materials (BOM) costs and their assembly costs.

2.1 Bill-of-Materials (BOM) costs

All the individual elements (optical, optoelectronic, mechanical and electrical), mount structures, subassemblies and packaging constitute an optical interconnect's BOM. BOM costs for photonic communication devices can represent a significant portion of the total cost for a device or optical interconnect. In general the larger the number of components or subassemblies the higher will be both the BOM cost and assembly cost. Historically tight alignment tolerance components have had a higher BOM and assembly cost.

An example of the large number of components in optical interconnects assemblies is to examine standard fiber connectors. Components in fiber connectors include precision tolerance ferrules and sleeves, mounting body, spring, and fiber boot.

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2.2 Assembly costs

Assembly costs for optical coupling methods are driven by optical component alignment tolerances with tighter tolerances being more costly. Optical component positional alignment tolerances can be divided into the different cost groups of: submicrometer, 1-5 !m, and greater than 10 !m. The capital cost of assembly process equipment is substantially greater and the processing time per alignment is longer for each smaller tolerance group, as detailed in Table 1.

Passive alignment of optical components provides for lower cost coupling than active alignment. In passive alignment, pick-and-place assembly equipment aligns components based upon fiducial marks without optical power coupling, monitoring or feedback control to the motion controller. Passive alignment times are much faster and are compatible with existing electronics industry automated assembly equipment.

Table 1. Assembly cost is driven by optical alignment tolerances.

Component Optical Alignment Tolerance (!m)	**Assembly Attachment Processing**	**Assembly Equipment**	**Assembly Time**
< 1 !m	Special Attachment Methods & Highly Skilled Process Set-up	Custom & Expensive	Slow
1 – 5 !m	Normal Die Attach Processing	Flip-Chip	Fast
10 – 20 !m	Normal Surface Mount Processing	Standard Surface Mount Automated Pick and Place Equipment	Very Fast

Assembly processing for optical interconnects often involves multiple assembly steps. For example, the assembly of fiber connectors, a butt coupling of optical fiber end faces, requires the assembly steps of: stripping off the fiber's protective buffer layer; inserting the fiber and adhesive into ferrules; curing the adhesive; polishing the ferrule/fiber end to a protrusion height and curvature specification; measuring the end fiber/ferrule end face shape; mounting the ferrule into a connector body with a precision ferrule bore, and spring load; applying adhesive to the connector body, fiber boot and fiber buffer and curing the adhesive. Assembly steps for active photonic devices such as a laser transmitter are much more involved consisting of multiple attachments of subassemblies, alignment and attachment of optical and optoelectronic elements and hermetic package processing.

2.3 Arrayed interconnects

One way to reduce the effective cost of optical interconnects is to configure arrays of interconnects in one coupling structure. Arrayed fiber connectors are available using SOB v-grooves and fiber ribbon configurations. Transponders using arrays of Vertical-Cavity-Surface-Emitting-Lasers (VCSEL) and arrays of photodetectors on one photonic chip have been used to lower interconnect costs in applications such as in 4 channel Coarse-Wavelength-Divison-Multiplexer (CWDM) transponders and have been explored for applications in board-to-board optical communication. Configurations of optical coupling to 2 dimensional arrays of VCSELs and photodetectors require custom connector interfaces. In arrayed interconnects fiber pluggability or "plug-and-play" configurations offer more value and deployment acceptance for their optical communications application markets.

A different approach to lowering optical interconnect costs by array design is to array all the active elements and multiplexing components into a single Photonic-Integrated-Circuit (PIC) and use a single optical interconnect for the high bandwidth wavelength division multiplexed (WDM) transponders. This lower cost WDM transponder approach has been deployed in InP based PICs [2] and in Si based PICs [3].

2.4 Low cost considerations

The following guidelines apply to configuring low cost options for optical interconnects:

1. Low cost bill-of-materials (BOM)
2. Fewer number of components and assembly process steps
3. High optical coupling efficiencies at high yield manufacturing
4. Larger alignment tolerances for assembly processes
5. Passive alignment rather than active alignment
6. Fast assembly processing times
7. Ability of fabrication methods to be scaled to high volume production rates
8. Compatibility with existing industry high volume assembly equipment and processing infrastructure

3. OPTICAL DESIGN

Optical design determines optical alignment tolerances. Assembly costs are determined by optical design and assembly processing design. Optical design choices include: butt coupling of similar sized waveguides; evanescent coupling along the waveguide skin length; and projection coupling.

Figure 1 schematically shows the two choices in optical design for projection coupling between two waveguides. If a single lens is used, submicrometer alignment tolerances are required for all components in two lateral axes (x, y) and micrometer tolerances in the depth axis (z). However, if two lenses are used there is no depth (z axis) sensitivity between the two lenses if the beam is collimated.

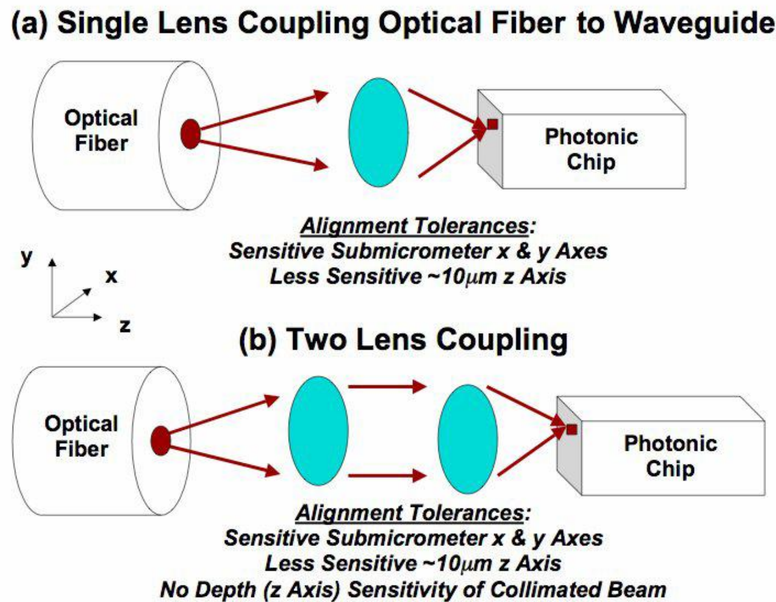

Fig. 1. Lens configurations for projection optical coupling of an optical fiber to a planar waveguide. (a) One lens, and (b) Two lenses.

4. LOW COST CONFIGURATIONS

This section describes a number of configurations that have advanced optical interconnects in terms of lowering cost. These configurations are presented in progressive order of lowering optical interconnect costs.

4.1 Silicon-Optical-Bench (SOB) and V-Groove butt coupling

SOBs provide a subassembly precision platform of well, platform and v-groove structures. SOBs lower assembly costs by enabling passive optical alignment of components and by reducing the number of parts to be assembled. SOBs are fabricated by wet KOH anisotropic etch of <100> silicon and are often pattern metallized for die attach and signal traces. SOBs are inexpensive and have been used in datacom transponders. A common configuration is to mount an edge emitting laser on a platform aligned to a v-groove for fiber alignment. The fiber is usually cleaved at a small angle and butt coupled to other photonic elements on the SOB.

Butt coupling of fibers placed in SOB v-grooves to etched facets of Planar-Lightwave-Circuit (PLC) waveguides has been a popular choice for coupling to FTTH transponders[4] and for coupling to silicon optical motherboard configurations postulated for chip-to-chip or board-to-board communication applications[5].

4.2 Ferruled fiber pluggable Transmitter-Optical-Sub-Assemblies (TOSA)

Another approach to lower optical interconnect costs is to reduce the number of components and to reduce the number of assembly steps by forming an integrated optical and mounting structure using the low cost scalable fabrication method of injection molding. The Transmitter-Optical-Sub-Assembly (TOSA) and associated Receiver-Optical-Sub-Assembly (ROSA) shown in Figure 2 has seen wide deployment. This design integrates a single lens into a mounting structure that has a precision bore for a pluggable ferruled fiber with an end stop, and a mounting structure for alignment and adhesive attachment to the top of hermetically sealed TO-can packages. The TO-can contains the active elements and their electrical connections. The TOSA body provides a pre-alignment of the lens to the inserted fiber. TOSAs are fabricated in plastic by injection molding with Ultem® being the plastic of choice. Injection molding is a fabrication method that is mature and scalable for high volume production. This scalability also has led to progressive reductions in price of injection molded TOSAs by a factor of 5X since their introduction. The development history of pluggable TOSAs is detailed in reference 6.

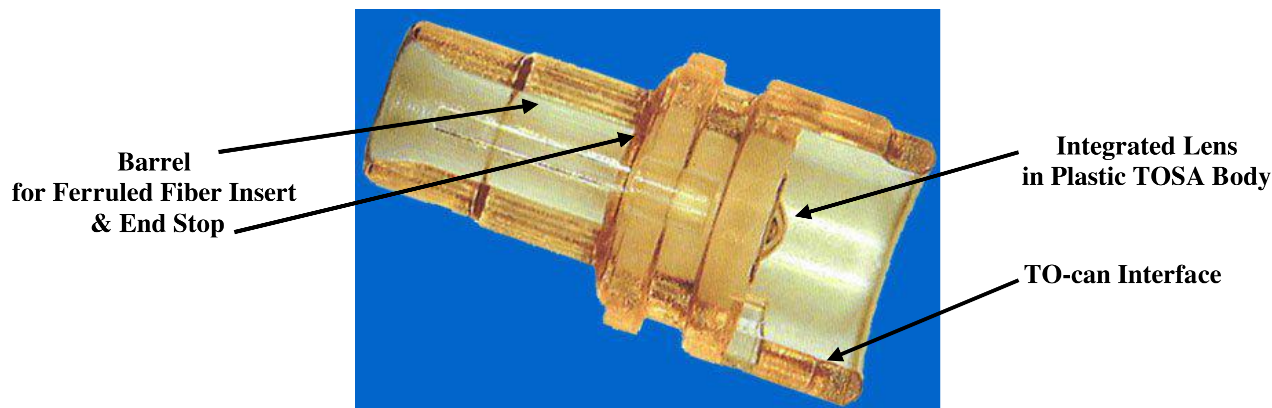

Fig. 2. Typical injection molded TOSA assembly. Ultem® plastic body incorporates a lens, barrel for ferruled fiber insert with barrel stop and mounting structure. Most frequently the plastic TOSA is glued to a TO-can laser package.

4.3 Evanescent coupling of lasers to PLC waveguides

Evanescent coupling of lasers to PLC waveguides has been made via a “Laser Surface Mount Converter” in the laser chip[4,7]. The laser chip is die bonded to a PLC top surface using passive alignment at ±2 !m alignment tolerance to PLC waveguides. This coupling attachment effectively seals the optical path, thus removing the need for hermetic packaging for laser reliability.

Evanescent coupling of planar waveguides to optical fiber is extremely difficult due to submicrometer tolerance control in removing fiber cladding and in maintaining evanescent contact distance with the planar waveguide.

4.4 Diffraction grating couplers

Optical coupling via scattering of light in diffraction gratings offers a method for low cost out-of-plane optical coupling. The gratings are low cost as they are lithographically aligned and are formed by wafer level etch processing. High refractive index contrast gratings and mirror metallization are required for high coupling efficiencies. Diffraction grating coupling efficiency is sensitive to light polarization and wavelength. Diffraction grating couplers have been implemented in silicon monolithic photonic circuits as “holographic lens” configurations at 1 !m alignment tolerance and with coupling efficiencies of up to -1.4dB (73%) into 0.1 !m^2 silicon-on-insulator (SOI) waveguides from optical fiber and from surface mounted lasers on the chip front-side[3]. This method works with both ridge waveguides and buried waveguides.

5. FUTURE DIRECTIONS FOR LOW COST OPTICAL INTERCONNECTS

Low cost optical interconnect developments are likely to use projection coupling across the photonic chip front-side and back-side. Optical alignment tolerances will continue to increase to greater than 1 !m to enable lower cost assembly align and attach processing.

Low cost designs are likely to utilize fabrication techniques such as injection molding of plastic optical subassemblies for fiber couplers. Characteristics of these subassemblies are could include integrated lenses and passive fiber alignment pigtail attachment. Optical couplers for fibers, laser chips or photodetector chips to planar waveguides may also include out-of-plane beam turning elements.

These low cost optical coupling solutions will be compatible with electronics industry standard surface mount assembly processing with passive optical alignment and fast attachment times.

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