Towards 100 % yield understanding approach in Lucent Technologies Madrid

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ABSTRACT

A wealth of advantages arise from breaking down the overall yield into yield components that are easier to work and closer to the manufacturing line environment. We present in this paper our strategy to attempt the 100% yield explanation on our fab and the process of building a pareto that quantifies the impact of each yield component (defects, probe, nothing found, etc...). The most critical one, the defect related, is accounted by a set of knowledge-based automatic software tools that operate in our fab. They quantify it and break it down into the by layer, by defect size and type (ADC) contributions. The step forward of communication and deployment of this yield strategy is a key topic also discussed in the paper. On our way towards the 100 % understanding of yield we have learned how to better manage it and taken advantage of many more opportunities to improve it. The strategy has shown to work both for new and mature technologies in our manufacturing line in Lucent Technologies Madrid.

1. INTRODUCTION

The attempt to understand which are the obstacles to achieve a 100% yield on each product is, indeed, too ambitious but, by aiming it we feel we are reaching a much better knowledge to manage a continuous yield improvement [1-7]. The combination of a set of intelligent data analysis software packages enables in our fab this yield model. Central one of this packages is Smartbit™, a bitmap to defect automatic correlate [8,9]. It provides information on yield loss by layer, defect size and ADC (automatic defect classification) type. This tool is complimentarily used with others to include in the yield pareto factors such as: wafer to wafer yield variations [10], process equipment to process equipment (being used for same step) yield variations [11,12], excursion rates, probe-test stability issues [13], etc...

With all this input sources a 100% yield pareto is built. The next steps are the formation of interdisciplinary teams around the top issues. Specific yield metrics, linked to the key processes, are chosen at every team. The status of the overall yield evolution and the team specific metrics are reviewed weekly. We present in this paper the process followed to implement the yield model described, together with the results obtained and the evaluation of the whole process.

We will structure the sections of this paper as follows. Section 2, titled yield metrics and components will introduce the question: what is yield?, and how do we measure yield?. We will describe how probe yield can be broken down into a set of yield components for tighter control and track. In section 3 we will focus our attention in the defect-related yield component, the most critical one. We will present the approach chosen to extract the contribution of each layer, process equipment and defect type to the overall defect yield component. Section 4 will deal with the communication and deployment phases of the yield components to the interdisciplinary teams that will drive them. On section 5 we present our evaluation of the 100% yield explanation model in our fab and summarize the main conclusions.

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2. Yield metrics and components

We will start with the view of yield we had years ago and then move to the present situation. In this way we intend to explain the reasons for the changes and the benefits of the evolution followed. Yield metrics have been mainly related to wafer probe: good devices per wafer, percentage of yield,... In order to compare the probe yields from different types of chips several defect density models (Poisson, Munro, Murphy,...) are used. This way to measure yield is very accurate but also reflects that the focus of the yield was located at the end of the manufacturing line. Yield reports, yield analysis tools and even yield meetings were based on probe yield. In-line data was merely a source of data to control processes and catch crisis, not still a way to measure yield. This situation had two basic problems: speed to detection and action was low and, probe yield metrics seemed too far away from daily process environment.

Our present approach is that probe yield can be broken down into a set of yield components. We define a yield component as any available source of data whose relation with final probe yield can be established in a systematic way. Within this definition, we have tried to find the widest variety of sources of data and developed software tools to extract the yield components out of them. As we were expanding our knowledge of the yield components, we have also learned how to best detect, measure and track each one of them independently. At this point, a key question came up to our yield team: does our set of yield components account for a nearly 100 % yield explanation?. The honest answer to this one is right now: "we are not still quite there but by aiming it we are taking advantage of many more yield opportunities and getting a deeper and closer understanding of the whole yield scope and how to manage it".

On Figure 1 we have represented schematically the process of breaking down the yield into smaller components.

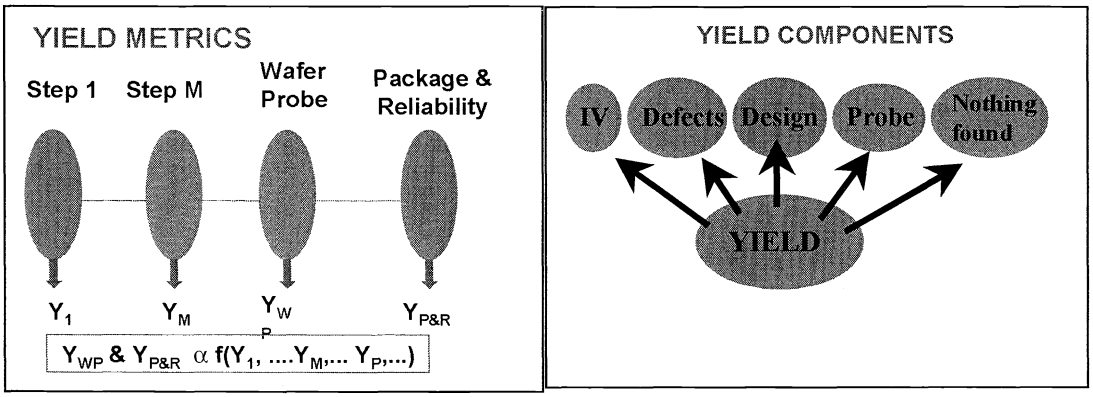

Figure 1: Yield metrics and yield components.

We now briefly present the set of yield components we currently handle at our fab: defects, final in-process testing (FIPT) or IV parametric testing, design, probe-test and nothing found.

The defect-related component is typically the largest contribution and will be covered in detail on section 3 of this paper. IV to wafer probe yield and IV to process parameter regressions and even spatial correlates are the tools commonly used to quantify the IV parameter yield component. This component tends to be more important at the beginning of a technology lifetime and critical on mixed-signal products. Design component is also a standard contribution to the yield that becomes key at prototype and initial product code lifetime. Comparison with other codes manufactured, correlates to IV, test characterization, physical failure analysis, etc, are tools typically used to detect and quantify design issues and verify if code requirements match current technology specs. Probe-test limited yield component is often not mentioned within the main set. According to our experience this is not a correct approach, specially for mature and mixed-signal technologies [13]. Software tools to match yield results among testers, to verify probe operation, to detect and retest probe bins out of statistical limits are very advisable. Procedures to probe wafers with a design tolerance experiment (DTE) before any new test program or test revision are also a healthy practice to prevent sporadic large yield excursions linked to the probe-test process. Last yield component, but not at all least important, is the nothing found contribution. It is a mandatory part of any

100 % yield explanation model to quantify and track the "nothing found". It is also advisable to continuously aim its reduction and its characterization in terms of: variability wafer to wafer, lot to lot, code to code, technology to technology, spatial distribution, ...

3. BY LAYER EXTRACTION OF DEFECT INDUCED YIELD LOSS

3.1 Localized defects

The defect yield component is, in most cases, the largest one and many different sources contribute to it. Every step along the manufacturing routing has a defect contribution in some extent. In order to detect and identify the defects added to the wafers, inspections are located in a set of selected steps of the line. Let us remind that inspection tools do not detect all the defects that kill a device, nor all defects produce a killed device. Therefore the correspondence between defects and killed devices is not straight forward.

In order to quantify the defect yield component and break it down into the by-layer contributions we have developed the software package Smartbit™. It consists in a bitmap to defect automatic correlate that provides information on yield loss by layer , defect size and defect class (through automatic defect classification ADCperformed at inspection tools). This correlation is performed in all our products having a RAM array built into them (around 25 to 40% of our load are DSP products). Details about architecture and functionality of this software can be found in reference [8]. Nevertheless we will present here the outputs that allow a quantification , understanding and track of the by layer defect yield loss. Smartbit™ can be useful for single wafers, lots and sets of any number of lots. (For the purpose of analyzing the yield behavior of a whole production line, a sample with a large enough number of lots is advisable) Just note here that in order to perform the bit failure to in-line detected defect correlate, the same wafers from the same lot-have to be inspected at every inspection step to allow adder calculation by level. In this way, for layer *i,* defects detected in all layers from 1 to *i-1* are subtracted to the ones detected at layer *i* and so on. A second note to take into account is that Automatic Defect Classification (ADC)has to be performed and stored at the inspection steps in order to link yield loss to defect class or nature.

In Figure 2 we display the main output from Smartbit™. This pareto provides the kill ratio by layer based on the amount of killed memory arrays linked to a defect detected by the inspection steps at each layer. The Nothing Found (NF) column is essential to evaluate the degree of confidence in the pareto (the lower the NF, the higher the defect yield component and the better the quality of our inspection steps). Actual NF values on our 0.3μ technology are in the range of 25-35%. The pie chart displayed for layer "POLY" gives us the weight of each ADC class from the POLY layer.

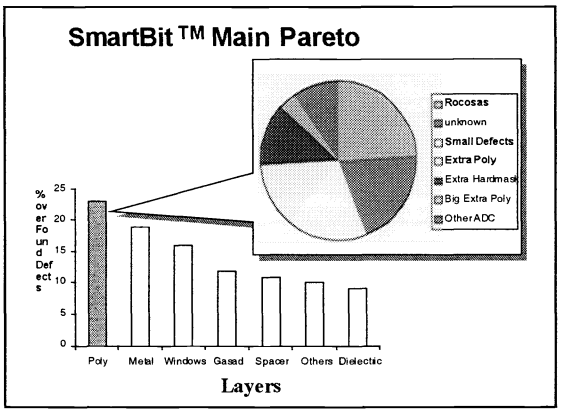

Figure 2: Main pareto from Smartbit™. Each column stands for the kill ratio of a layer. The pie contains the contributions of different defect classes (ADC) to one of the layers.

Once we know the weight of every layer on the defect yield loss we need as much information about each layer defects as possible. Smartbit™ provides a wide variety (over 50 different ones) of output types that came out of the needs of our yield analysts for the last 2 years. They include trends, spatial distributions, paretos, ... with information from layers, defect sizes, defect types (ADC), bitmap signatures and more. By looking and combining them, one gets a fairly deep understanding on each killer defect at every layer. On Figure 3 we have displayed a representative set of them. A more detailed information on Smartbit™ can be found in reference [8].

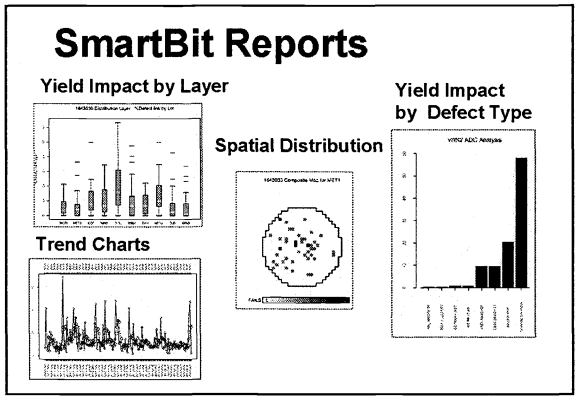

Figure 3: Set of output reports from Smartbit™. It includes trends, spatial distributions and paretos.

We have seen in this section 3.1 how defect yield component is broken down into by layer, by defect size, by defect class subcomponents. At this point, one can quantify each one of them, track each one of them and set independent goals to each one of them. This makes the yield improvement projects a task closer to the organizations that make it possible: operations, process engineering, equipment engineering, defect inspection and yield analysts. Another advantage, that will be highlighted later on, is that we have enough information to prioritize our defect fighting activities ordered by yield impact.

3.2 Localized and non localized defects

As mentioned above not all the defects that kill are detected by the inspection tools, due to the lack of detectivity or to the sample size inspected. Therefore other tools have to be used complementarily with Smartbit™ in order to lower the NF position of the defect yield component and reach closer to the 100% yield explanation. In this sub-section we present two in-house software packages named Posiscan™ and Toolscan that account for two key yield components: wafer to wafer yield variations within a lot (Posiscan™ software) and process tool to process tool yield variations (Toolscan software). See references [1,3,10,11,12] for a more detailed information.

Depending on how mature the production line is, wafer to wafer yield variations may be as relevant as lot to lot yield variations. A track of these two sources of yield variability is needed to understand the dominant sources of yield loss. This task can be accomplished with an statistical analysis of within lot yield distributions and lot to lot (average) yield distributions. They can be quite different for different product codes and different technologies, and this can be advantageously used to try to understand why and to match them to the one having tighter yield distribution.

Wafer to wafer variation within a lot is often dominated by the effect of just one of the steps of the fabrication routing. In this particular, "killing step" , wafers may have been processed sequentially one by one, or in a multichamber tool, or whole lot a time, etc... For instance, if one of the chambers of a four-chamber process tool is the one impacting yield, just one fourth of wafers will have lower yield. If we record wafer processing order (bar-code reading) in this tool we will obtain a relation between wafer number and yield. In the same way, we could relate yield loss to other types of process tools. Within this scope we developed a software to correlate processing order versus yield. Yield losses produced in different tools can have a kind of "footprint" that we called order patterns (see in Figure 4 examples of order patterns).

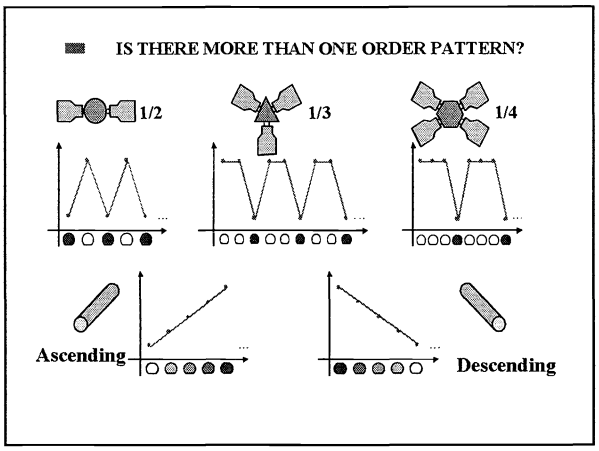

Figure 4: Examples of typical order patterns that are found on lots: ½ (one evry two wafers is worse), 1/3 (one every three wafers bad), descending (degrading yield tendency wafer to wafer), etc...

We have accumulated a wealth of experience on dealing with order patterns and developed algorithms to automatically detect them on every lot probed. Posiscan™ is the knowledge-based software package developed to automate the analysis and detection of order patterns. A brief note here: if wafer order remains nearly unaltered throughout the whole routing, an order pattern could be originated in any of the process tools of the same kind. To reduce the scope for the search of killing tool, reading and randomization steps are located along the routing. In this way , the number of possible "killing steps" is reduced from the whole routing into smaller subsets (that we call "modules"), as many as the number of read/randomize steps we have. Time to root cause detection of wafer to wafer (within-lot) yield variation is, in this way, dramatically reduced. On Figure 5 we display the main output from Posiscan™ , which consists on a table with lot identification, order pattern detected, "module" of the manufacturing line where the pattern was found and degree of confidence of the classification. This report is automatically generated for every lot right after being tested at wafer probe.

Posiscan™ Main Report

LOT	MODULE	PATTERN	DEGREE OF CONFIDENCE
7183-55000	ILD 2	½ Ascending	91% 71%
7137-55000	ILD2	½	87%
7137-55000	METAL 3	¼	73%
7701-55000	ILD2	½	90%

Figure 5: Main Posiscan™ output table.

The process tool to process tool yield variations (given they perform the same step) is often significant. We should continuously attempt to match the yield performance of all our tools to the best in class for each step of the routing. A step

by step comparison is time consuming and not worthy. In our case, we developed Toolscan, a software that automatically compares (using statistical tests) the yield performance of process tools for each step of the routing. It provides an output list of those steps with differences statistically significant among tools. Boxplots and trend charts of suspicious steps can then be viewed within the tool. From the routinely use of Toolscan, an estimation of the process tool to process tool yield variation component can be attempted. The practice of matching all process tools to the best one, for each type of tool and process step, is a continuous source of yield improvement.

4. YIELD COMMUNICATION AND DEPLOYMENT

We have discussed on previous sections the advantages of breaking down the overall yield into components that are easier to work with and closer to the daily manufacturing line environment. We have also described how this goal is currently attempted in our fab, by the use of a set of knowledge-based automatic software tools. We now have a pareto quantifying the impact of each yield component (defects, probe, nothing found, etc) and also the information on how defect yield component is broken down into by-layer, by size and type (ADC) contributions (with the outputs from Smartbit™, Posiscan™ and Toolscan described on section 3).

The question is now: how do we actually communicate and deploy this yield strategy into the manufacturing line to make it work in a fast and efficient way?. Up to this point, the main responsibilities were kept inside the yield enhancement organization (defect detection, probe yield analysis, in-line technologists and failure analysis). This was just an initial step, yield does not improve by analyzing it. Next step was the communication to the rest of the organizations involved on yield (process & equipment engineering, operations, test,...). Top yield hitters were discussed and a reduced set of them were selected for deeper work. This step is critical and tends to be driven by yield impact, resources and success chances. The step forward in the deployment of this yield strategy in our fab was the formation of the reduced set of interdisciplinary teams involving the organizations and persons actually needed from different organizations: process engineers, equipment engineers, test engineers, operations, yield and defect analysts, etc... We have called them as "baseline teams". Each baseline team is focused on a specific yield component and has its low-level (ad-hoc) yield metric. This baseline teams organization is dynamic, as yield is. Lifetimes of each team will be different, depending upon obstacles, yield impact, etc... On Figure 6 we display schematically the process of yield communication and deployment followed at our fab.

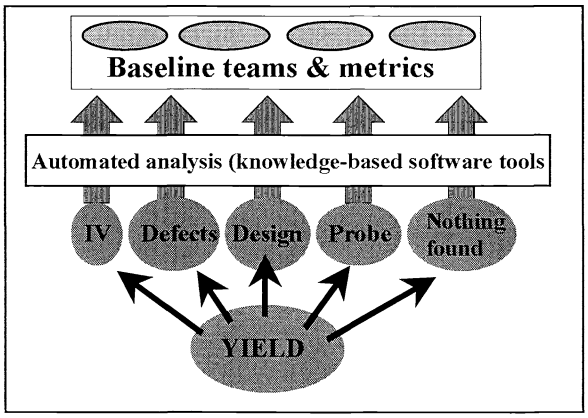

Figure 6: Schematics of the yield deployment.

As seen in Figure 6 the metrics of each baseline team must be directly related to the overall probe yield. Goals for each metric have a predicted impact on probe yield and the sum of the impacts of every team should be consistent to the yield goal for the company. We have set up a weekly review meetings for the baseline teams and a by-weekly meeting to review and report the progress of overall yield and its components. It is our feeling that now yield , yield metrics and yield improvements are getting much closer to all organizations involved than it was before attempting the yield strategy described in this paper.

Last, but most important, the yield improvement that is being achieved in our fab using this approach is remarkably good. It has shown to be valuable for fast ramp-up of new technology and also to accelerate the improvements on mature technologies. On Figure 7 we display a yield evolution (in d0 chart) for the ramp-up of a technology. It should be noted how yield achieved goals soon and then continued improving.

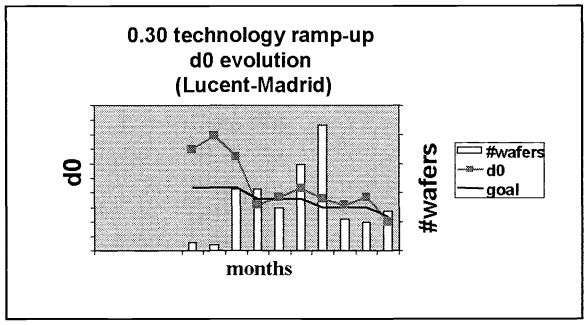

Figure 7: Yield evolution (expressed in d0) in the ramp-up of the 0.3 microns technology. Squares are monthly average d0, thin line is d0 goal and columns are wafer volume per month. Note that as wafer volume increases, d0 learning curve improves too

5. CONCLUSIONS

We have described our strategy to attempt the 100% yield explanation on our fab. We have discussed the advantages of breaking down the overall probe yield into components that are easier to work and closer to the manufacturing line environment. We have described the process of building a pareto that quantifies the impact of each yield component (defects, probe, nothing found, etc...). We have presented a set of knowledge-based automatic software tools that operate in our fab. They deal with the most critical yield component , the defect related, and break it down into the by layer, by defect size and type (ADC) contributions. The step forward of communication and deployment of this yield strategy has been also noted as a key.

On our way towards the 100 % understanding of yield we have learned how to better manage it and taken advantage of many more opportunities to improve it. The strategy has shown to work both for new and mature technologies in our manufacturing line in Lucent Technologies Madrid.

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REFERENCES

[1] M.Recio, "Strategy and tools for yield enhancement" Proceedings on SPIE´s Microelectronics Manufacturing Technologies: Yield, Reliability and Failure Analysis. Edinburgh, May 1999, EUROPTO Series.

[2] M.S. Effron, "Integrated yield management: systematic approach to yield management". ASMC, 397, Nov. 1996.

[3] M. Recio, J. Moreno, M.A. Merino, J.A. Ayucar, V. Martín and A. Godino, "Fast and efficient yield entitlement for 0.3 microns technology production ramp-up". Proceedings on SPIE´s Microelectronics Manufacturing Technologies: Yield, Reliability and Failure Analysis. Edinburgh, May 1999, EUROPTO Series.

[4] C.H. Satpper and R.J. Rosner, "Integrated circuit yield management and analysis: development and implementation". IEEE Trans. on Semiconductor Manufacturing, vol 8, No 2 , 95-102, May 1995.

[5] S.P. Cunningham, C.J. Spanos and k. Voros, "Semiconductor yield improvement: results and best practices". IEEE trans on Semiconductor Manufacturing, vol 8, No 2, pp103-109, May 1995.

[6] C. Gondran, "A technique for measuring and improving yield team performance". Yield Management Seminar Proceedings, KLA Yield Manufacturing Series, Austin TX, 1996.

[7] F. Lee, "Advanced yield enhancement: integrated yield analysis". ASMC, pp67-75, Sept 1997.

[8] M.A. Merino, S. Cruceta, A. García, M. Recio, "Smartbit™ bitmap to defect correlation software for yield improvement" (in press). Proceedings of ASMC Conference. September 2000. Boston MA.
& U.S. Patent " " No

[9] A. Fernández, A. Urquía, M. Recio, V. Martín, F. Vega, A. Riloba, et al, "Bitmap in multimodule IC as a tool for baseline failure analysis". Proceedings on 20th Int. Symp. For Test and Failure Analysis, pp.267-272, 1994.

[10] M.A. Merino, M. Recio, J. Moreno, V. Martín, A, Fernández, G. González et al, "Yield improvement via automatic analysis of wafer processing order". Proceedings on SPIE´s Microelectronic Manufacturing Symp., vol. 3510, pp. 135-146, 1998.
& U.S. Patent No 60/096,407 "Method and system for analyzing wafer processing order"

[11] M. Recio, A. Fernández, V. Martín, M.J. Pemán, J.R. Hoyer, S. Whitlock et al, "Advanced software system for yield improvement in manufacturing fab". Proceedings on SPIE´s Microelectronic Manufacturing Symp. , vol. 2874, pp. 219-229, 1996.

[12] V. Martín, M. Recio, M.A. Merino, J. Moreno, G. González, G. Sanchez et al, "Knowledge-based software system for fast yield loss detection in a semiconductor fab". Proceedings on SPIE´s Microelectronic Manufacturing Symp., vol. 3216, pp. 88-101, 1997.

[13] E. Rodriguez, C. Cano, J. Sanchez-Vicente and J. Moreno, "Wafer probe process verification tools". (in press) Proceedings on 2000 ASMC. Boston MA. Sept 2000.