Evolution of semiconductor process technology

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ABSTRACT

For the past 30 years the number of transistors integrated into a single chip has doubled every one to two years; that trend has not slowed down. Actually, it has accelerated every time we hit a technology barrier point (1μm,0.5μm,0.25μm and now .1μm). New developments in process and equipment technology have enabled us to follow Moore's law to reduce the average dimension of the physical features of integrated circuits from 10μm (1970s) down to .1μm (2001). What will be the limit be? 0.01μm and 120"? We will not reach it within this decade.

INTRODUCTION

In the early 1980's, 1μm technology was seen as a barrier, as was 0.5μm technology in the late 80's and 0.25 μm technology in the early 90's. Today, we're at 0.1μm. And, wafer sizes have gone from 4" to 6" to 8" to 12". What will the limit be (fundamentally and practically)? We do not know, but the pace has not slowed. However, it is getting increasingly difficult and for each new generation there have been more obstacles. For the 0.1μm generation, there are several obstacles: 248nm to 193nm for lithography, thin gate oxides, low-resistance gates, high k capacitors (Ta_2O_5), Cu interconnect, low k, high aspect ratio contacts and trench etching, not to mention transition from 8" to 12" wafer size.

1. PHOTOLITHOGRAPHY

In the early 1980s, it was predicted that optical lithography would run out of steam, and that x-ray lithography would be required beyond 1.0um. Now, with new advances in planarization, photoresist, reticles, optics, light sources, and process technology, optical lithography is alive and well. The industry pushed I-line lithography (365nm) to produce 0.25μm features through the use of attenuated phase-shifting masks, CMP, and improved resist. Advances in chemically-amplified photoresist and excimer laser technology made lithography at 248nm wavelength possible. Due to continuing improvements in photoresist performance and in mask layout and fabrication, 248nm lithography will be used for the mass production of 0.13μm design rule chips. With progress in phase-shift mask, better optical systems, and refined stage technology, 0.11μm lithography at λ=248nm is not out of the realm of possibility. Today the trend in wavelength reduction continues with the introduction of 193nm lithography, which requires high quality (and quantity) CaF_2 for optical systems and new photoresist chemistry. Preliminary data indicates that 193nm lithography can be used to resolve sub-0.09μm features. Optical lithography doesn't stop here! Several companies have announced 157nm programs designed to deliver features as small as 0.07μm. Beyond 0.07μm, the industry will have to choose between emerging non-optical lithography techniques, which include projection 1x x-ray lithography, projection ion beam, projection e-beam lithography and extreme-UV lithography (optical!!!).

2. ETCH

From Wet etch in the early 1970's, we've progressed from parallel plate plasma reactors to RIE, MERIE and to today's High-Density Plasma sources. Moore's law (fig#1 graph of Technology node vs year) has held true for horizontal dimension (i.e.: gate W/L); however, there is no law for the vertical dimension. The vertical shrinking has been slower causing the increase in contact height; contact aspect ratio has increased from less than 1 in the early 1980's to more than 15 to 1! "High density" plasma sources were developed by decoupling the plasma generation power from the control of ion energy at the wafer, resulting in higher plasma density without necessarily producing high energy bombardment at the wafer surface. Higher etch rates and good selectivity control, together with minimal resist erosion were achieved to enable etching >20:1 aspect ratio contacts with minimal damage. For some oxide etch applications, the trend in the industry is swinging back to "low density" and "medium density" etch systems. Along with all of the benefits that were provided by high density oxide etch systems, there also came problems such as narrow process windows for profile control. The goal moving forward is to keep the benefits which were gained by the move to high density while decreasing the sensitivity of the processes to variation in the etch parameters. However, in applications such as polysilicon and metal etching, the high density plasma sources remain quite strong in their process performance.

Coupling with tighter overlay requirements, the use of Self-aligned contacts (SAC) has been widely used (Fig#2 Micron's 64M cross section) using a high density plasma source and chemistry having oxide to nitride selectivity greater than 20:1, which was unimaginable 10 years ago.

In *Challenges in Process Integration and Device Technology*, David Burnett, Shin'ichiro Kimura, Bhanwar Singh, Editors, Proceedings of SPIE Vol. 4181 (2000) • 0277-786X/00/$15.00

For 0.1um technology, new etch chemistries, together with new etch sources, will be needed for thinner 193nm photoresist, higher aspect ratio contacts, thinner gate dielectrics and electrodes, and exotics materials (W/WN/Pt/Ru).

3. DIFFUSION

Batch Furnaces started as horizontal quartz tubes that were manually fed. Wafers were loaded onto quartz boats and the quartz boats were then loaded onto the trays which were slid into the tube (hand pushed rod!!). As wafers progressed to 8 inches and processes demanded tighter process control limits and ambient control, the furnaces advanced to a vertical layout with automation. This purge became a necessity with thin nitrides beginning approx. in the 0.35 um technology due to the growth of an interfacial oxide during the push pre-cell nitride deposition. This ambient control is also very important now for tungsten word-line processing.

Todays vertical furnaces have built in stockers fully automated with advanced model based temperature control +/- 1C and ability to ramp up >100C/min and ramp down >50C/min. The advantage of fast ramp can be seen in short process times at higher temperatures such as gate oxide. However, the true advantage of fast ramp systems may be in the temperature control capability of the systems. Cross-wafer uniformity can be controlled by rapidly cycling the heating core temperature. Temperature control and wafer temperature modeling are beginning to be very important for critical processes. These issues will be paramount at 300mm. (fast ramped furnaces); These new development will be needed for precise temperature controlled required for .1um technology where junction is <0.1um . With thinner gate and cell capacitor, interface control is the key for increase performance. Many suppliers have decided to trade of batch size for performance by introducing mini-batch furnace and single wafer.

4. RTP

The state of the art RTP system 6 years ago was essentially one robot feeding one chamber with no ambient control for the wafers prior to insertion into the heating chamber. No wafer rotation was used. Temperature control was virtually non-existent.

Due to backside emissivity, the pyrometer shipped with the system for temperature control would be disconnected for better process control.

New developments in emissivity independent temperature measurement for RTP together with better temperature control by rotation and multizone lamp control have been instrumental in bringing RTP to mainstream manufacturing.

5. CVD

As aspect ratios increase with shrinking, trench and contact become deeper and harder to filled. Several material filling methods are used for advanced technology: HDP oxide used for trenches; CVD Si_3N_4/Ta_2O_5 used for cell dielectrics, CVD TiN/W used for contact filled. Recently, Atomic Layer Chemical Vapor Deposition (ALCVD) is introduced; in an ALCVD process each chemical is introduced seperately into the reaction chamber one at a time; The chemical is reacted layer at a time; therefore the name ALCVD. Due to layer by layer deposition process, the ALCVD deposited film is very uniformed, has excellent step coverage and low in defects; However, the deposition process is very slow.

6. CMP

Fourteen years ago, CMP was considered a black magic rather than a science. The tool set and consumables were very primitive: the wafer was pushed against a hard pad with dripping diluted silica slurry with brush and scrapper used for cleaning up the pad. After the wafer is polished (others would call it a grinding process!!). The polishing rate would change from wafer to wafer. If you were lucky, you would have a good pad (tested by feeling it with your hand) and the scratches would be acceptable.

Today CMP technology has improved with the introduction of advanced carrier with multizone pressure control, new pad technology and insitu metrology allowed better process control; However, pad conditioning still required (new pad has better repeatability of pad conditioning or decreased sensitivity to pad conditioning)

Even with 2nd generation hardware however CMP still suffers from a process repeatability issue which is still largely related to pads and pad conditioning. As a result from several years ago efforts have started to replace conventional pads with Web technology (roll to roll) that does not require pad conditioning. The consumable of choice in this regard is the 3M fixed abrasive pad which in addition to alleviating the need for pad conditioning provides improved planarity of the end product. The web approach also can enable extremely long pad life which will further improve the manufacturability of CMP

7. DEVICES

Looking forward there will be many changes and hence challenges in the semiconductor device areas. At 0.1 um features size, operating voltage will be reduced to around 1V-1.5V. To maintain certain device threshold voltage to control off-current, which is critical in such products as DRAMs, will severely limit the transistor current drive and therefore the system speed at such low voltage level. SiO_2 or nitrided-SiO_2 gate dielectric thickness will continue scale to 1-2nm. New high-K gate dielectric materials such as Al_2O_3, HfO_2, ZrO_2 Ta_2O_5 are closer to reality but their trapping characteristics and sensitivity to hot-electrons are remained to be seen. Ultra-shallow junctions (~200A) made possible by ultra-low energy implant (less than a few keV) and plasma doping will further curtail subthreshold leakage however, how to control hot electron-induced damage and gate-induced drain junction leakage will be a difficult task. New emerging technologies like SOI, SiGe will start to play a bigger role in special applications but conventional Si-based substrate material will continue to be the dominant material on which most semiconductor devices will be built.

8. CONCLUSION

By following Moore's law, the semiconductor industry has changed our societies with ever shrinking devices; We have not reached the limit yet, but there are many more obstacles as we continue down to sub 0.1um (yes, it is 0.1um not 1um) for all technology fronts: Photo, etch diffusion, CVD, CMP, clean. New technologies are emerging to enable us to shrink both horizontal and vertical dimensions; what will the limit be? 0.01um and 120"? (Si roll?)

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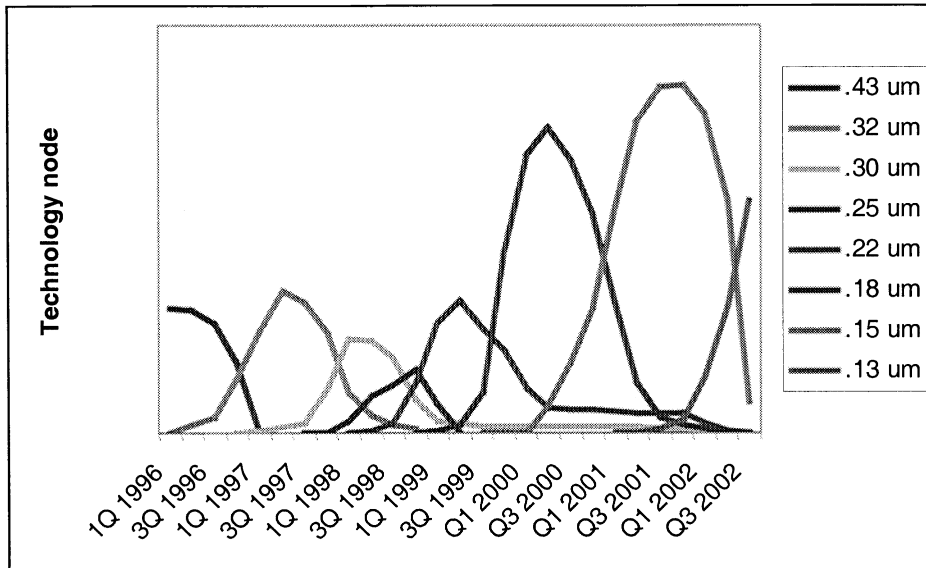
Fig#1 Technology node vs year



Fig#2 Micron's 64Meg cross section