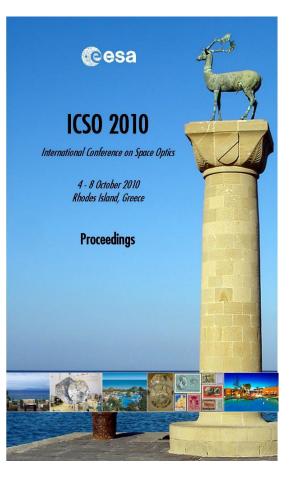# International Conference on Space Optics—ICSO 2010

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High performance photonic ADC for space applications

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HIGH PERFORMANCE PHOTONIC ADC FOR SPACE APPLICATIONS

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I.   INTRODUCTION

The flexibility required for future telecom payloads will require of more digital processing capabilities, moving from conventional analogue repeaters to more advanced and efficient analog subsystems or DSP-based solutions. Aggregate data throughputs will have to be handled onboard, creating the need for effective, ADC/DSP and DSP/DAC high speed links. Broadband payloads will have to receive, route and retransmit hundreds of channels and need to be designed so as to meet such requirements of larger bandwidth, system transparency and flexibility.[1][2]

One important device in these new architectures is analog to digital converter (ADC) and its equivalent digital to analog converter (DAC). These will be the in/out interface for the use of digital processing in order to provide flexible beam to beam connectivity and variable bandwidth allocation.

For telecom payloads having a large number of feeds and thus a large number of converters the mass and consumption of the mixer stage has become significant. Moreover, the inclusion of ADCs in the payload presents new trade-offs in design (jitter, quantization noise, ambiguity). This paper deals with an alternative solution of these two main problems with the exploitation of photonic techniques.

II.   CONVENTIONAL A/D CONVERSION

Mainly, an electronic ADC must carry out two functions over a time-varying signal. On the one hand, it samples the signal and holds it for a period of time, on the other, quantifies those samples in a certain number of levels. To do so, two important parameters are taken into account: the sampling period and the number of levels. The number of levels is set by the number of bits of the specific ADC. As a general rule, the ADCs behaviour gets worse both for amplitude and timing errors, being the jitter the most important one for timing errors and the thermal noise and non-linearities the most important one for amplitude errors. All these error sources deteriorate the *effective number of bits* (ENOB) in the ADC. [3]

There is a great range of parameters to be taken into account in analog to digital conversion, and the ENOB is probably the most representative. The above mentioned parameter is affected by some factors like timing jitter and amplitude noise among other things. Throughout the years, the sampling rate in conventional electronic ADCs has been constantly increased. However, this increase in sampling rate involves a reduction in resolution [4].

In Fig. 1, the achieved ENOB for a wide range of ADCs is displayed, being plotted in accordance with the analog input frequency. It is important to notice the limits imposed in this graph. Since the ideality in components that would be necessary for making high performance ADCs is not achievable in many occasions, the product bandwidth-dynamic range is limited by physical and technological constraints:

- Noise contributions (thermal, shot, flicker …) integrated over the sampling period.
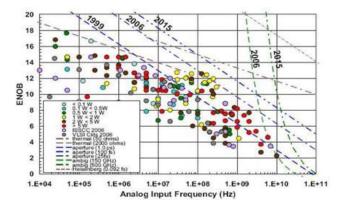- Jitter. The uncertainty due to the clock phase noise, which affects the maximum input frequency.

Fig. 1. Electronic ADCs review [4]

Mainly, the ADC conventional electronic architectures include Nyquist frequency ADCs, subsampling-based ADCs and multichannel architectures [3]. Subsampling-based ADCs combine the subsampling with additional processing techniques to reduce quantization noise. In this way, resolution improves with regard to Nyquist frequency ADCs, although at the expense of bandwidth. Multichannel architectures use N parallel ADCs instead of one ADC. These architectures are used for extending the ADCs performance to higher sampling frequency applications. Nevertheless, multichannel architectures involve bigger physical structures, and misalignments between channels degrade resolution as well.

The sub-sampling schemes perform a downconversion of the original signal without any external mixing by exploiting the periodic characteristics of the sampling physic. In these systems, the radio-frequency signal is directly sampled by an Analog-to-Digital (ADC) converter with a sample rate lower than the maximum frequency of the signal. The ideal condition in this case is that the bandwidth of the signal to be sub-sampled has to satisfy the Nyquist condition of $2 \cdot BW < Fs$, being BW the pass-band signal bandwidth and Fs the sampling frequency, in order to avoid ambiguity in the downconversion process.

The key parameter in this case is the analogue input bandwidth of the ADC, which should be greater than the carrier frequency. Typically, for an electronic ADC, this parameter is related to the sample-and-hold circuit that captures the signal previously to the electronic quantization. Usually, the input bandwidth of an ADC is greater than its Nyquist frequency (Fs/2), although not enough for digitalizing high frequency signals as the required in this project (for example E2V EV10AQ190 or National Instruments ADC12D1800). One option in these cases is the use of external track-and-hold (TH) circuits especially designed for sub-sampling operation. Nevertheless, these circuits, as the internal sample-and-holds of the ADC, introduce distortion resulting in a significant decrease of the dynamic range and the effective number of bits (ENOB) for higher frequencies.

Other alternative to be able to digitize the bandpass signal, is the use of downconversion which use a mixer and a local oscillator to beat this last signal with the incoming signal. After a filtering, the original signal is "converted" from RF (K-band, Ka-band …) to IF (Intermediate Frequency) where the E-ADC is able to work. Conventional analogue downconversion techniques exhibit also some limitations like the LO leakage, the image rejection or require the use of different downconversion and filtering stages (super-heterodyne configuration). If the application requires multiple branches, there will be limitations in size, mass (limited by mechanical isolations for avoiding EMI and leakage effects) and consumption. Table 1 depicts one example for 200 channel RF downconverter (information available in the Thales Alenia Space web page concerning standard single-channel downconverters):

Table 1: Mass/Consumption estimation for 200 channel downconversion

RF down conversion system estimation for 200 channels			
	Ka stage	**IF stage**	**Down conversion total**
Size	2500x400x400 mm3	2000x160x250 mm3	
Volume	400 l	80 l	~500 l
Mass	120 kg	60 kg	~180 kg
Consumption	800 W	800 W	1.6 kW

III.   PHOTONICS IN SPACE APPLICATIONS

The concept of a photonic satellite where optical subsystems reduce the microwave and digital electronics complexity on-board communications spacecraft is considered very attractive for its potential to reduce the mass and volume of a payload requiring increased processing bandwidth. Use of on-board photonic subsystems could therefore render advanced Satcom systems cost-competitive with respect to alternative technologies.

Photonically-assisted ADCs (PADC) can offer significant advantages to the standard all-electronic approach by using photonic sampling with ultra-low jitter pulses for superior performance. Moreover, by optically subsampling the signal a direct downconversion can be performed at the same stage, obtaining substantial improvements in performance by achieving a very precise sampling of the signals thanks to the ultra-low jitter of the pulsed lasers, a signal downconversion without mixing and conversion stages, reducing the spurious and the LO leakage and saving mass, volume and complexity thanks to the use of distributed architectures and fiber optic remote delivery, especially in the proposed scenario in which hundreds of digitalizers are required.

In Fig. 2, the scheme of implementation of the future telecom payloads with 100-200 ADCs with the traditional solution (frequency converters) and with Electro-photonic ADCs is depicted. [7]

In this paper, the overall objective is to presents a laboratory demonstrator of a photonically-assisted ADC and to verify its performance including some environmental tests, as well as suggest a development roadmap for this technology for its application in future telecom satellite payloads.

The electro-photonic ADCs must be capable of sub-sampling analog signal in the Ka band (29.5 GHz) with an input bandwidth up to 2 GHz with a sample rate lower than 1.5 Gbps. This enables the direct digital downconversion of channels in the Ka band up to 1.5GHz/2 = 750 MHz in a transparent way. The optical sampling subsystem previous to the electronic quantification should be optimized in order to achieve the best performance in term of Signal to Noise Ratio (SNR) and Spurious Free Dynamic Range (SFDR).

IV.   PADC: DIFFERENT ARCHITECTURES

In general, there are four main classes of photonic ADCs: 1) photonic assisted ADC in which a photonic device is added to an electronic ADC to improve performance, 2) photonic sampling and electronic quantizing ADC, 3) electronic sampling and photonic quantizing ADC, and 4) photonic sampling and quantizing ADC. An excellent review of the state-of-the-art of almost all the photonic ADCs schemes is described by Valley in [6], including the trade-offs and main characteristics.
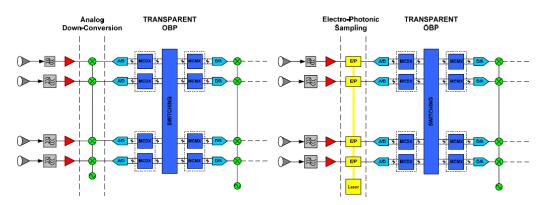

Fig 2. Scheme of implementation of the future telecom payloads with 100-200 ADCs with the traditional solution (frequency converters) (left) and with Electro-photonic ADCs (right).

The one based on using femtosecond pulsed laser, electro-optical modulation based on Lithium-Niobate Mach-Zehnder interferomenters and electronic quantization employing electronics ADC is especially interesting due to it exhibits the best trade-off of performance in terms of capability of high-precision sampling (low jitter, low noise) required for high frequencies, input bandwidth (related to the electro-

optical modulator), the use of optical fiber very interesting in distributed systems, maturity of the components, easiness of implementation and reliability, especially in the case of on-board space.

This kind of structures is based on modulating a temporal train of quasi-deltas by the input signal. This temporal deltas, after the modulation, carries the amplitude of the original signal in a concrete instant. When this train is photodetected, these amplitudes are quantized by an ADC, resulting in a photonic-assisted analog-to-digital conversion process.

A more complex scheme is based on this previous architecture and exploits the wavelength division multiplexing for implementing a parallel scheme in which the optical samples are time de-interleaved and detected-and-quantized by different receptors. The parallel samples are serialized for constructing the original sampled signal. Although this scheme is potentially very powerful, since high sample rate can be achieved, the practical difficulties in its implementation such as the skew and equalization limits the maximum achievable ENOB. Due to this reason, the baseline for implementing the sub-sampling ADC is the simple scheme but with improvements in order to exploit the maximum capabilities from all the components.

Although this scheme has been intensively analyzed in the literature, some key aspects are yet not solved in the literature in order to achieve the optimum performance of the sampling process, which is limited at the end by the jitter effect. The jitter is the random error that occurs in the sampling process (the signal is not sampled in the ideal time but in a moment slightly different) and translate in a superposed noise in the sampled signal that limit the effective number of bits.

V.   DEMONSTRATOR IMPLEMENTATION

As can be appreciated in Fig. 4, an optical train of low jitter ultrashort optical pulses which will be used as the sampling signal is generated by the Femtosecond Pulse Laser (FPL) with 1.3 GHz of Pulse Repetition Frequency (PRF) (a mode-locked laser configured in free-space working in 1550 nm). This optical signal travels through the fiber to the subsampling subsystem, which is mainly comprised of a dual-output Mach-Zehnder modulator and some circuitry maintaining its working point in ideal conditions (even for extreme environmental conditions). For this application, special photo-detectors with high-bandwidth and high linearity in a differential configuration are used for optimum performance. The optical processing is important because it enables to manage much higher mean power at the photodiode optimizing the dynamic range of the system. After being photo-detected, a stage of amplification and filtering adapts the signal to the ADC. One of the key elements in this architecture is the optical source, since the quality of the optical pulses is directly translated into the quality of the output signal under quasi-jitter limited working conditions. Jitter, which is very low but noticeable at high frequencies, and optical noise are the limiting factors.
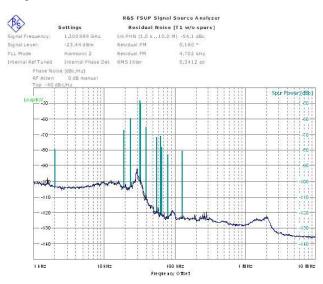

Fig. 3: Phase Noise of the Pulsed Laser with low RMS Jitter 341 fs (integrated from 1 KHz to 10 MHz)
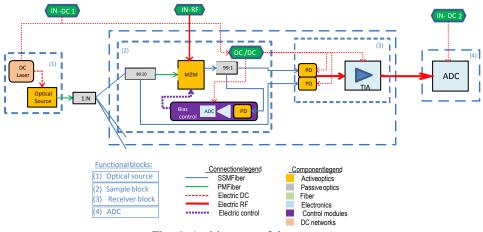
Fig. 4. Architecture of the system

VI.   PRELIMINARY RESULTS

The following results were obtained implementing the system described with only one branch (the splitting ratio was emulated by adding insertion loss). The simulation provides the following results for a total loss of 18.3 dB. That means a 1:8 splitting ratio in order to use several ADC with the same system, all using the same optical source. The results are presented in Fig. 5 were the spectrum at the output of Transimpedance Amplifier (TIA) and the digitalized signal are shown. Additionally, Table 2 contains the most relevant parameters. These values will be validated during the next stages of the project but are reliable for this case. Simulations and measurements have been included which were used to validate the simulation software. In fig. 6 captions of a sampled signal has been included, both in its temporal and the frequency forms. The measurements correspond to a sampling system working at 1.3 GHz, with a total optical losses of 24.5 dB, an amplitude modulation from a 130 MHz signal, and detected with a photoreceiver integrating a photodiode and a TIA (Rtia = 800 Ohm) working in a linear regime. The bandwidth of this measurement (hold filter) was of 3.5 GHz.
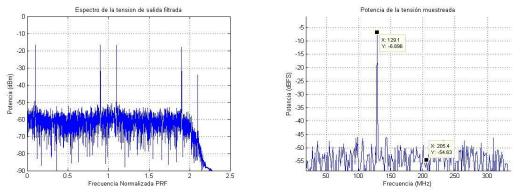

Fig. 5: Spectrum at TIA's output and at ADC digitalized output

Table 2: Measured parameters for 1:8 splitting (8 digitizers)

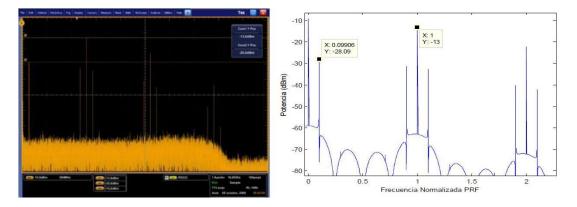| Pout (dBFS)	Noise (dBm/Hz)	Gain (dB)	SNR (dB/MHz)	SFDR (dBc)
-6,89	-117,9	21,11	49	70

Fig. 6 Measured and simulated output

VII. CONCLUSIONS

In this paper, a photonic assisted ADC has been presented. It consisted in femtosecond pulsed laser with ultralow jitter addition. With the adequate architecture and the most suitable optical components the circuit can be used in several ADC in order to increase the capacity of the payload. Some others additional architectures were presented, which were discarded in favour of the most interesting in terms of performance, cost and complexity.

Considering the mass, volume and consumption figures, and when comparing with an example of implementation with real proven RF hardware (see Table 1), the photonic design described here present a high gain in this figures. Initial estimations show an improvement higher than 200%, especially in consumption and mass (high mass gain can be obtained when the RF waveguides and cables are replaced by optical fibre).

The simulation made and the measures presented seem very promising, given that they achieve performances similar to conventional analogue systems with reduced complexity, size, mass and consumption.

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