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Substrate integrated micro-thermoelectric coolers in glass substrate for next-generation photonic packages

Parnika Gupta,* Amit Tanwar, Xiuyun He, Kamil Gradkowski, Kafil M. Razeeb, Padraic E. Morrissey, and Peter O'Brien*

University College Cork, Tyndall National Institute, Cork, Ireland

ABSTRACT. Managing the temperature of photonic chips within intricate electro-optic packages poses a notable challenge concerning the thermal crosstalk between the photonic chip, electronic chip, and the chip–fiber connection point. This is a multifaceted problem and requires packaging solutions that cannot only address high-performance thermal management but must also be scalable to high volumes. Glass has long been thought of as a suitable platform for next-generation photonic packaging due to its low thermal conductivity, which minimizes unwanted heat transfer between electronic and photonic components. Achieving proper thermal isolation between the chips and the chip–fiber interface necessitates a microscale thermal solution that guarantees accurate temperature regulation of the photonic circuitry without disrupting the optical coupling interface with the fiber array, due to the presence of epoxy used for fiber attachment. We propose a technique for the development of a substrate-integrated microthermoelectric cooler (SimTEC) for the effective temperature control of the electronic and photonic integrated devices. The proposed device uses glass substrate vias that are half-filled with p and n-type thermoelectric materials and the other half with copper. A COMSOL multiphysics model is developed to study the variations in the cooling performance of this SimTEC device based on changes in the via parameters. Interestingly, the maximum range of temperature gradient variation for SimTEC is 6 times greater compared to that of equivalent free-standing micro-TEC pillars. However, there are some challenges associated with implementing this method, as the temperature gradient (or cooling effect) achieved by SimTEC still falls short of that achieved by the free-standing micro-TEC pillars.

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1 Introduction

As we progress toward high-bandwidth communication networks, the succeeding generation of photonic packages demands enhanced levels of integration between electronics and photonics within a system-in-package architecture.[1,2] With closely packed electronic and photonic elements, there arises a thermal interplay between the electronic and photonic chips, potentially impacting temperature-sensitive optical functionalities within the photonic chip. To counteract this thermal interaction and uphold mechanical stability, glass substrates (low coefficient of

*Address all correspondence to Parnika Gupta, parnika.gupta@tyndall.ie; Peter O'Brien, peter.obrien@tyndall.ie

thermal expansion 3.25×10^{-6} K^{-1}) have emerged as a viable solution due to their limited lateral heat propagation.[3] Glass substrates also exhibit favorable electrical and optical routing characteristics, featuring a low loss tangent and the suitability for optical waveguide/micro-optical integration.[4] High-density electrical connections can be created within glass through the use of redistribution layers, microvias, and through-glass vias (TGVs).[3,5] This dense electrical routing facilitates the close integration of electronic and photonic chips, leading to minimal electrical transmission loss between these components.[6] However, this also introduces another challenge in thermal management—the heat generated by electronic chips must be dissipated within the glass package. TGVs filled with copper serve as a passive cooling solution to manage the heat generated by electronic chips.[7–9]

For photonic chips, specific optical elements, such as ring resonator filters, modulators, and semiconductor optical amplifiers are sensitive to changes in temperature, as they operate at specific wavelengths. As a result, the temperature sensitive components on the photonic chips necessitate thermal control capabilities to counteract the impact of temperature fluctuations in the operating environment, thereby maintaining optimal performance.[10] One solution for thermal stabilization involves the integration of centimeter-scale thermoelectric coolers (Macro-TEC) at the bottom of the package, as illustrated in Fig. 1(a). Nonetheless, variations in temperature by the macro-TEC can cause different package components and materials—such as electronic chips, photonic chips, solder bumps, underfill, and epoxies—to deform in distinct ways, potentially affecting the optical coupling between the photonic chip and the fiber.[1,10] An alternate approach involves achieving precise thermal control of photonic components through the use of free-standing micro-thermoelectric coolers (micro-TEC). These micro-TECs are compact, lightweight, compatible with CMOS fabrication, and result in lower material consumption. They allow for direct on-chip cooling when the chip is bonded face-up on a substrate.[2,11] However, this requires additional packaging steps, including the bonding of the micro-TEC module onto the chip and attaching a heat sink to the hot side junction of the micro-TEC.

When the electronic/photonic chips are flip-chip bonded (face-down) onto the glass substrate, integrating a micro-TEC on the chip involves adhering the micro-TEC device to the backside of the photonic/electronic chips. This introduces parasitic thermal resistance due to the chip's thickness, as depicted in Fig. 1(b). Recent discussions by Zhang et al.[12] have delved into the optimization of a micro-TEC embedded within a cavity etched in the thermal interface material (TIM) layer atop a 3D integrated architecture and this setup connects to a heat spreader layer. Nevertheless, challenges emerge when photonic and electronic chips within a 2.5D configuration possess different thicknesses, leading to varying thicknesses of the TIM layer connected to the heat spreader.[13] This necessitates the redesign and fabrication of the micro-TEC

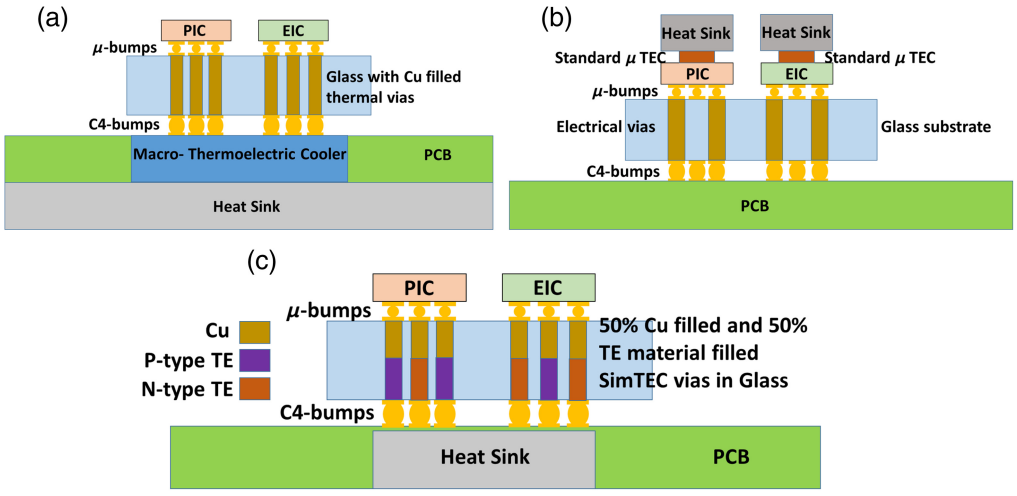

Fig. 1 Schematic showing different approaches of thermoelectric cooler integration in a photonic package where photonic integrated chip (PIC) and electronic integrated chip (EIC) are co-packaged together on a glass substrate where the implementation of (a) macro-thermoelectric cooler (Macro-TEC); (b) micro-TEC (μ-TEC); and (c) SimTEC in photonic packages is highlighted.

with distinct thicknesses for effective thermal control of the photonic and electronic chips. One strategy to mitigate this challenge involves embedding the micro-TEC within a cavity in the substrate. However, this approach introduces additional complexities, such as die shifting, costs related to precise trench fabrication, precision in die embedding, and integration of the heat sink mechanism connected to the embedded micro-TEC's hot end.

Thereby, in this paper, we propose a strategy that involves employing TGVs as thermoelectric cooler (TEC) pillars. In this approach, the vias are filled with copper and thermoelectric materials through electroplating. This innovative method is referred to as substrate integrated micro-TEC (SimTEC), highlighted in Fig. 1(c). SimTEC facilitates targeted and precise thermal management of photonic chips, enhancing thermal connectivity with the surface of the photonic chip (which is bonded face-down onto the substrate) and maintaining a compact form factor for the glass package. Further reduction in thermal resistance at the chip surface and the cold-side TEC interface can be achieved by transitioning from microbump and underfill-based bonding to copper–copper (Cu–Cu) hybrid bonding. In this case, the heat sink can be integrated with the printed circuit board, similar to the architecture of macro-TECs as shown in Fig. 2. The thermal design is intricately linked with the substrate design, wherein the glass substrate can be divided into domains for signal transmission, power transmission, passive, and active thermal management. Notably, this approach eliminates the additional fabrication cost associated with micro-TECs, offering designers greater flexibility in customizing substrate thermal design to accommodate variations in areas corresponding to chip regions requiring thermal adjustment. As described by Mahajan et al.,[14] the maximum temperature limits for the photonic and electronic chips within a photonic engine are delineated distinctly along with changing ambient temperature of the package. This distinction renders the SimTEC approach a viable method for precisely adjusting the chip temperature, complementing broader system-level thermal management techniques. A parallel scenario arises in the neuromorphic photonic accelerator module,[15] where specific components, including the core photonic processor, DFB lasers, and SOAs, are susceptible to thermal fluctuations. This susceptibility presents an opportunity for the SimTEC device to provide a temperature stabilization solution seamlessly integrated into the module. Furthermore, SimTEC can be applied to achieve thermal stabilization in quantum photonic devices with exceptional accuracy during prototype development.[16] Although this integrated architecture enables localized temperature control, the presence of a glass substrate around segmented vias increases the thermal response time due to the heightened thermal mass of the device.[17]

Earlier efforts by researchers have demonstrated the application of polymer-embedded micro-TECs, showing a net cooling temperature (9.6 K), serving as a chemically stable packaging technique for thermoelectric pillars.[17] However, the compatibility of these embedded micro-TECs with solder reflow processes has not been explored. Liu et al. also examined the fabrication and performance analysis of a thermoelectric generator based on through glass pillars

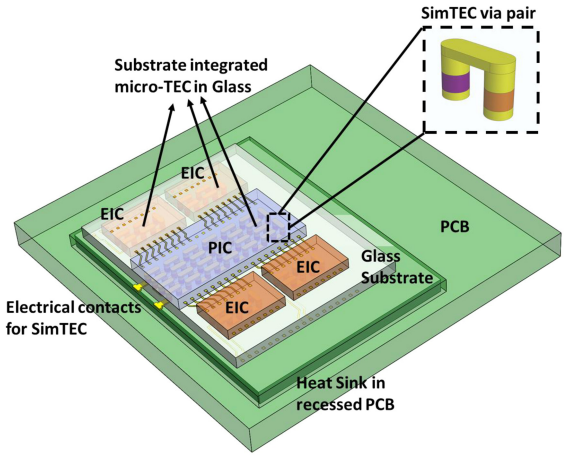

Fig. 2 Diagram showing the SimTEC architecture in glass substrate with the SimTEC vias operating in the central region of the EIC and PIC with the chip's peripheral *I*/*O*s dedicated for electrical connection in the photonic package.

Table 1 Features of a centimeter scale TEC (Macro-TEC), free-standing micro-TEC device, and SimTEC.

	Macro-TEC	Micro-TEC	SimTEC
Temperature cooled (K)	60 to 80	10 to 20	~10
Size	Centimeter	Micrometer	Micrometer
Fabrication complexity	Low	High	High
Device stability	High	Low	High
Flip-chip compatibility	Low	High	High
Thermal resistance between chip surface and TEC cold-side surface	High	Moderate	Low

for the recovery of low-grade waste heat. This setup generated a maximum output voltage of 40.89 mV under a temperature difference of 138 K.[18] The advantages attributed to thermoelectric legs integrated into glass pillars, including increased leg height of the thermoelectric pillars, operation resistant to oxidation and moisture, established manufacturing processes for creating through holes, and cost-effectiveness of glass compared to photoresist, have been elaborated upon.[18,19] These advantages also extend to the SimTEC approach, where the focus is on achieving controlled temperature operations of the TEC.

The performance of a thermoelectric module is based on the efficiency of the thermoelectric materials and the design parameters for the TEC. The performance of the thermoelectric materials is measured by $zT = S^2\sigma\kappa^{-1}$, where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity, and T is the absolute temperature.[11,19] As discussed in the literature, the electroplating technique is considered for the deposition of thermoelectric materials in unfilled TGVs.[2,11,19] There are various techniques for the formation of TGVs that can be considered for the fabrication of SimTEC, such as mechanical drilling, wet drilling, laser drilling, sandblasting, inductively coupled plasma etching, discharge methods, and glass reflow methods.[20] The formation of TGVs is then followed by electrodeposition of the copper and thermoelectric materials in the TGVs and the formation of copper interconnects on the top and bottom of the glass substrate.[18] The performance of the TEC module is also impacted by the design parameters of the thermoelectric legs or the TGV parameters in the case of SimTEC.

In this work, we have theoretically investigated the impact of variation of via parameters, such as via diameter, via height, via pitch and fill factor of deposited copper and thermoelectric materials in the via on the cooling performance of SimTEC. This cooling performance is simulated as the surface temperature difference between the hot side interconnect (where heat is dissipated from the bottom of the glass substrate) and the cold side interconnect (where heat is absorbed from the top of the glass substrate) with the application of a current. This cooling mode can also be converted to the heating mode when we reverse the polarity of the applied current, thus enabling localized thermal tuning of the photonic chips. We have simulated a thermoelectric via pair using finite-element method analysis in COMSOL Multiphysics® software. The thermoelectric via pair in SimTEC is also compared with the free-standing thermoelectric leg pair with the same parameter variations to highlight the impact of the glass substrate on the thermoelectric performance. A further optimization analysis for the diameter, height and pitch of the TGVs has been done to see the cooling performance of the SimTEC and free-standing thermoelectric leg pair. Table 1 tabulates the features of a macro-TEC, micro-TEC, and SimTEC for briefly differentiating the feasibility of the three thermal tuning approaches in photonic packaging.[21]

2 Simulation Approach

A thermoelectric module consists of p-type and n-type leg pairs, which are arranged alternatively, such that they are electrically connected in a series configuration and thermally connected in a parallel configuration.[22] SimTEC consists of a via pair in glass, where one via is filled with copper and p-type thermoelectric material and the other via is filled with copper and n-type

thermoelectric material. A DC current is applied to the copper interconnect connected to the n-type via side and the interconnect on the p-type via side is connected to ground. This current flow gives rise to a temperature difference between the top and bottom copper interconnects of the glass with vias because of the Peltier effect.[11]

Considering the isotropic properties of the materials, the continuity equation for the electric current density in a thermoelectric module is given by[23]

$$\Delta \cdot J = 0,$$

where J is the electric current density.

This current density in the TEC is dependent on the Ohm's law and the Seebeck effect, which is given by[23,24]

$$J = -\sigma(\Delta V + S\Delta T), \quad E = \frac{J}{\sigma + S\Delta T}.$$

Similarly, the heat flux generated in the TEC can be divided into the effect of the Joule heating and the Seebeck effect, which is translated as[11,24]

$$q = STJ - \kappa\Delta T,$$

where σ is the thermoelectric material's electrical conductivity, S is the Seebeck coefficient, κ is the thermal conductivity of the thermoelectric material, and T is the absolute temperature.

The steady-state equation for heat transfer is given by[11,23]

$$-\Delta \cdot q + q' = 0, \quad q' = J \cdot E = \frac{J^2}{\sigma} + J \cdot ST.$$

Thus the three-dimensional model that governs the thermoelectric effects in the simulation model is expressed as[11,24]

$$\Delta(\kappa\Delta T) + \frac{J^2}{\sigma} - TJ \cdot \left[\left(\frac{\partial S}{\partial T}\right)\Delta T + (\Delta S)_T\right] = 0,$$

where the first term on the left-hand side denotes Fourier heat conduction due to temperature difference, the second term stands for the Joule heat, and the third term represents the temperature dependent effects of thermoelectric materials (Thomson effect). Assuming a steady-state condition, where the Thomson effect of thermoelectric materials, contact resistances, heat losses by conduction, and convection are not taken into account; the cooling power (Qc) for a single thermoelectric leg pair is given as[11,24]

$$Q_c = (S_p - S_n)T_c I - \frac{1}{2}I^2R - K(T_H - T_c),$$

where S_p and S_n denote the Seebeck coefficient for p- and n-type materials, respectively; T_H and T_C denote the temperature on the hot side and cold side, respectively, I is the applied current, R is the electrical resistance of the leg pair ($R = \rho L/A$) and K denotes the thermal conductance of the leg pair ($K = \kappa A/L$). The symbols ρ, κ, L, and A denote the electrical resistivity, thermal conductivity, length of leg pair, and cross-sectional area of the leg pair, respectively. In the equation for cooling power, the second term which stands for the Joule heat and the third term which stands for the Fourier heat conduction play a significant part and are affected by the geometric parameters of the thermoelectric leg pair.[11] Hence, the thermoelectric leg geometry parametrization and its impact on a free-standing thermoelectric leg pair and a SimTEC via pair integrated in the glass substrate are investigated in the next section.

The simulation model for a free-standing TEC leg pair consists of a p-type leg and an n-type leg half filled with copper and half filled with thermoelectric materials. Electrodeposited BiSbTe and Bi_2Te_3 are considered as the p-type and n-type thermoelectric materials, respectively, in the simulation. The top and bottom interconnect is considered as 3 μm thick copper traces. An aluminum heat sink is connected to the hot-side of the TEC, which is electrically isolated from the bottom traces with a thin layer of aluminum dioxide. Electrical contact resistance (R_c) at the copper and thermoelectric material interfaces is considered as 1×10^{-11} Ωm^2.[26,27] Thermal contact resistance and heat losses by convection and radiation are not included in the simulation

Table 2 Thermoelectric properties of the materials measured at room temperature.

Materials	Thermoelectric properties			Ref.
	Seebeck coefficient (μV/K)	Electrical conductivity (S/m $\times 10^6$)	Thermal conductivity (W/m K)	
BiSbTe (p-type TE)	90.5	0.026	0.6	25
Bi_2Te_3 (n-type TE)	−121	0.052	0.85	26
Copper	1.5	59.6	398	
Glass	Electrically isolated	Electrically isolated	1.2	
Aluminum dioxide	Electrically isolated	Electrically isolated	30	
Aluminum	Electrically isolated	Electrically isolated	237	

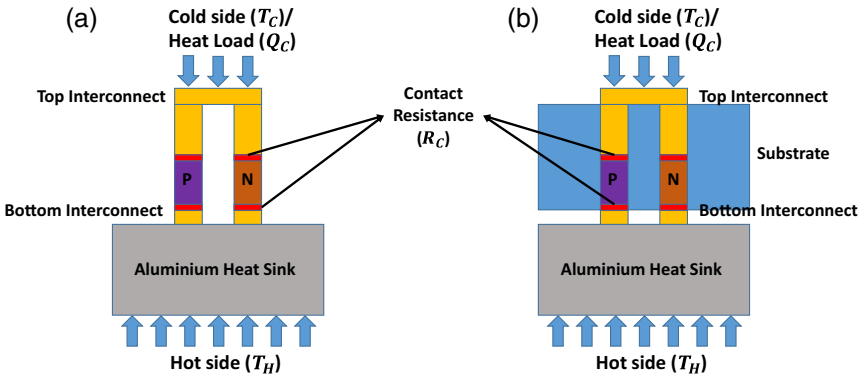

Fig. 3 Simulation model for (a) free-standing micro-TEC leg pair and (b) SimTEC via pair.

model for simplification. In the case of SimTEC, the simulation model remains the same with the addition of glass substrate around the p-type and n-type vias, such that glass is thermally connected to the vias but electrically isolated from the current flowing through the vias and the copper interconnects (Table 2). The initial parameters in the simulation model are 30 μm diameter, 60 μm pitch, and 100 μm height of the cylindrical leg pair/via pair. The fabrication of free-standing micro-TEC pillars with height >20 μm becomes extremely difficult and we are using the simulation models of the free-standing micro-TEC pillars in this paper for an equivalent comparison with SimTEC device performance. The height of the glass substrate is kept the same as the via height. Simulation parameters in a single via pair, such as via diameter, via height, via pitch, and fill factor (filling ratio of thermoelectric material and copper) are investigated in the case of SimTEC and compared with the equivalent free-standing micro-TEC leg pair case. The simulation model for free-standing micro-TEC pillars and SimTEC vias is shown in Fig. 3.

3 Results and Discussions

3.1 Substrate Integrated Micro-TEC

In this study, three different substrates, glass, silicon, and air, with their thermal conductivities 1.2, 148, and 0.02 W/mK, respectively, are chosen in order to see the influence on cooling performance of the thermoelectric cooler. Figure 4 shows the temperature gradient (ΔT) of free-standing TEC and segmented TEC for three different substrate materials. In this case for both SimTEC and free-standing micro-TEC pillars, the via diameter, via pitch, and via height are considered as 30, 60, and 100 μm, respectively. These geometric characteristics are made possible by employing thin glass manufacturing, laser-assisted via creation within the glass, and successful electroplating of both copper and thermoelectric materials. These combined efforts

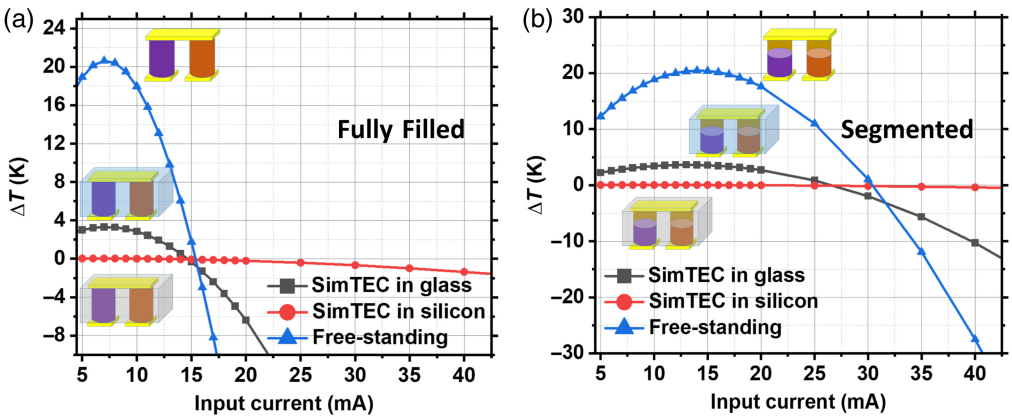

Fig. 4 Graphs showing the change in temperature gradient in the case of a SimTEC when the substrate is varied between glass, silicon, and the case where the micro-TEC pillars are free-standing (no substrate). This variation in cooling capability is highlighted in both conditions when the vias/pillars are (a) fully filled with thermoelectric material and (b) when they are segmented, i.e., half-filled with thermoelectric material and half-filled with copper.

ultimately play a role in reducing the overall package size.[28–30] As the input current is increased in Figs. 4(a) and 4(b), the temperature gradient of fully filled and partially filled segmented SimTEC in glass substrate increases to a maximum value of 3.314 and 3.629 K, respectively, due to the combined Peltier and Fourier effects, followed by which ΔT starts decreasing due to the overpowering joule heating effect (I^2R). In the case of both segmented and fully filled devices, the ΔT across the SimTEC device is significantly less than that of the free-standing micro-TEC. For example, the ΔT in the case of segmented free-standing micro-TEC is 20.45 K, whereas the ΔT in the case of segmented SimTEC vias is only 3.629 K (~6 times lesser than 20.45 K). This is because of the substrate material, which is in physical contact with the pillars and provides an additional heat dissipation path. In other words, the substrate allows a part of the heat to be transferred through heat conduction and decreases the temperature difference between the top and bottom copper interconnects on the substrate. As expected, the increase in thermal conductivity of the substrate material leads to a further decrease in thermal resistance and lends a thermal shunt path through the substrate. As a result, the ΔT keeps decreasing as thermal conductivity of the substrate material increases, with approximately no cooling for the silicon substrate because of the high thermal conductivity of silicon substrate (148 W/mK). The simulation results highlighting the temperature distribution across the free-standing micro-TEC pillars, SimTEC vias in glass substrate, and SimTEC vias in silicon substrate are shown in Fig. 5. This figure also clearly shows the decrease in the temperature gradient across the top and bottom interconnects of the TEC from Figs. 5(a)–5(c), which is perpetuated due to the thermal losses in glass and silicon substrates.

The input current corresponding to maximum ΔT in the case of fully filled vias is lower (approximately halved) as compared to that of the segmented vias in the case of both SimTEC and free-standing micro-TEC pillars. This is due to the increased electrical resistance and thermal resistance for the vias fully filled with thermoelectric material as compared to the segmented vias half-filled with copper and half-filled with thermoelectric material. The input optimum current in Fig. 4(a) corresponding to maximum ΔT increases from 6 mA in the case of SimTEC with silicon substrate to 7 mA in case of both SimTEC with glass and free-standing micro-TEC. Similarly, the input current in Figs. 4(b) and 5 corresponding to maximum ΔT increases from 9 mA in the case of SimTEC with silicon substrate to 13 mA in case of SimTEC with glass to 14 mA in the case of free-standing micro-TEC. Based on the results, glass is a superior material for SimTEC as compared to silicon. It allows the temperature control of the micro-TEC over a broader range of input currents. The cooling capacity Q_c, which is the maximum heat that can be effectively dissipated from the surface of a thermoelectric device, is calculated in Table 3. As shown in Table 3, the cooling power (also mentioned in Sec. 2) of the segmented pillars/vias is higher than that of the fully filled thermoelectric material filled pillars/vias (for approximately similar ΔT_{max}) because of the increase in operating current corresponding to maximum cooling.

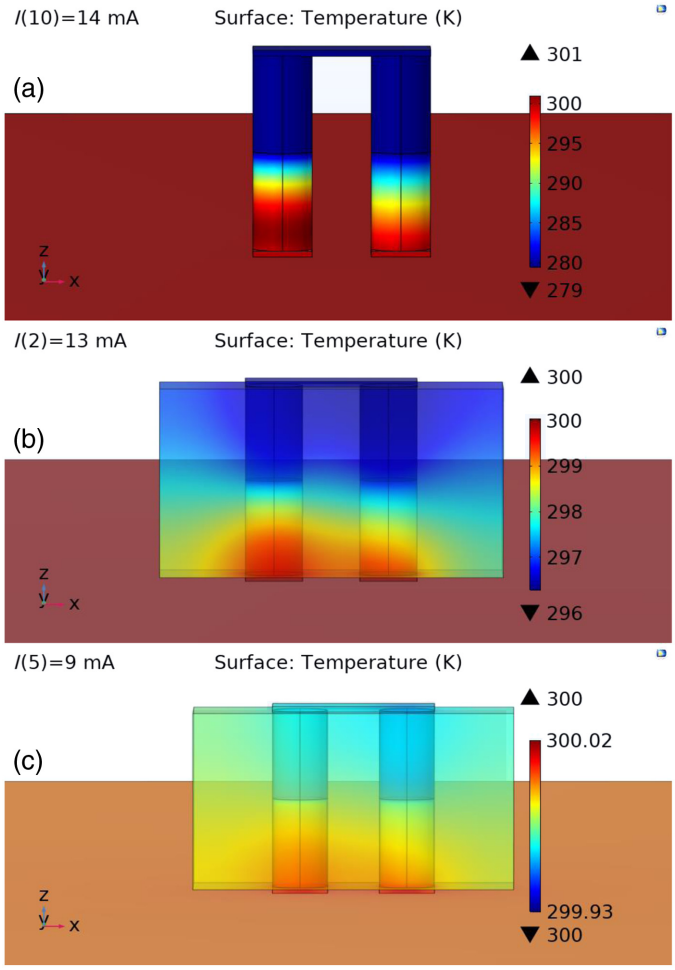

Fig. 5 Simulation results showing the temperature gradient across the top and bottom interconnects in the case of (a) free-standing micro-TEC pillars, (b) SimTEC vias in glass substrate, and (c) SimTEC vias in silicon substrate, showing the thermal losses substrate is contributing to the decrease in maximum temperature gradient across the TEC.

Table 3 Cooling capacity of fully filled and segmented pillars/vias in free-standing and SimTEC configurations when $\Delta T = \Delta T_{max}$.

	Q_c (mW)	
	Fully filled	Segmented
SimTEC in glass	0.2036	0.3898
SimTEC in silicon	0.2321	0.4019
Free-standing micro-TEC	0.000504	0.002652

The cooling capacity in the case of fully filled free-standing micro-TEC pillars is the smallest (approaching zero) as it is operating at maximum ΔT.

3.2 Effect of SimTEC via Diameter

In the case of both free-standing micro-TEC pillars and SimTEC in glass substrate, the via/pillar diameter is increased from 30 to 50 μm, whereas the pitch and via/pillar height is kept constant at 60 and 100 μm, respectively. Figures 6(a) and 6(b) show the effect of increasing leg diameter in

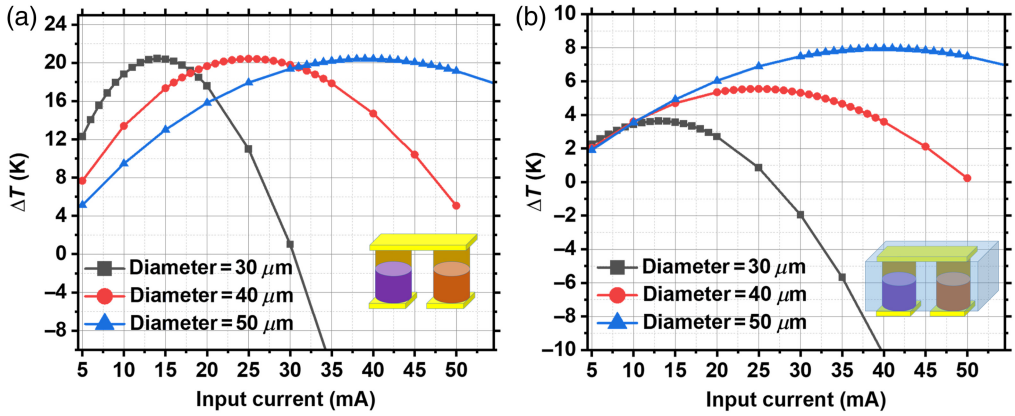

Fig. 6 Graphs showing the change in temperature gradient in the case of (a) free-standing micro-TEC pillars and (b) SimTEC vias in glass when the diameter of the vias/pillars partially filled with copper/thermoelectric material is varied from 30 to 50 μm, when the pitch and height of the vias/pillars are kept constant.

Table 4 Cooling capacity of free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T = \Delta T_{max}$ for different pillar/via diameters.

	Q_c (mW)	
Diameter (μm)	Free-standing micro-TEC	SimTEC in glass
30	0.002652	0.3898
40	0.004917	0.6248
50	0.007419	0.8207

free-standing micro-TEC and increasing via diameter in SimTEC on temperature gradient. As discussed in the last section, the temperature gradient initially goes up and then goes down with applied current because of the combined effects of the Peltier effect, Fourier heat, and Joule heating. The increase in pillars diameter in the case of free-standing micro-TEC leads to a decrease in electrical resistance, but it also implies that the thermal conductance of the device would increase. These two opposing phenomena lead to a drop in ΔT. However, in the case of glass SimTEC as the via diameter increases, the temperature gradient across the device increases steadily. The SimTEC with diameter 50 μm shows the maximum ΔT of 7.96 K, which is approximately double as compared to that of the SimTEC with the diameter of 30 μm. As the diameter of the vias is increasing, the gap between the vias becomes smaller, which means that there is smaller volume of glass between the vias. This decreasing volume of glass between the vias limits the thermal leakage in the glass substrate between the vias and hence an increase in device cooling performance.

The cooling performance of the free-standing micro-TEC is better as compared to SimTEC because of no thermal losses (thermal shunt) in the glass substrate. In both Figs. 6(a) and 6(b), the input current corresponding to the maximum cooling of the TEC increases with increasing diameter because of the decreasing overall electrical resistance of the device. The current values for the corresponding maximum ΔT remain approximately same in both free-standing micro-TEC and SimTEC, because of the same electrical resistance of the device. The cooling capacity, as shown in Table 4, in both cases increase with the increase in diameter of pillars/vias due to the decrease in both electrical and thermal resistance of the device. The reduced electrical resistance leads to a decrease in the joule heat (I^2R) distribution to the cold end.

3.3 Effect of SimTEC via Height

In this study, both free-standing micro-TEC pillars and the segmented via/pillar height of the SimTEC in glass is increased from 50 to 100 μm, whereas the segmented via/pillar diameter,

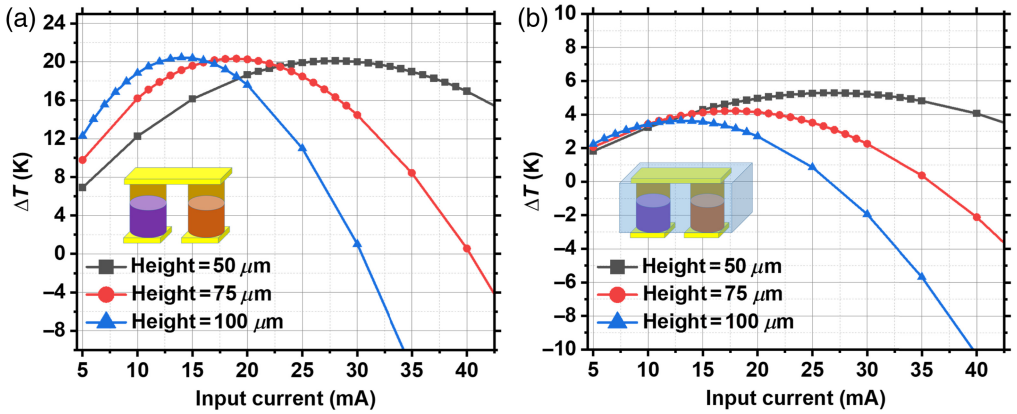

Fig. 7 Graphs showing the change in temperature gradient in the case of (a) free-standing micro-TEC pillars and (b) SimTEC vias when the height of the vias/pillars partially filled with copper/thermoelectric material is varied from 50 to 100 μm, when the pitch and diameter of the vias/pillars are kept constant.

Table 5 Cooling capacity of free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T = \Delta T_{max}$ for different pillar/via heights.

	Q_c (mW)	
Height (μm)	Free-standing micro-TEC	SimTEC in glass
50	0.008074	0.6977
75	0.004257	0.5041
100	0.002652	0.3898

pitch, and fill factor are kept constant at 30 μm, 60 μm, and 0.5, respectively. The height of the pillars is a crucial factor for the cooling performance of the TEC device, as the height influences both the electrical resistance and thermal conductance of the device. In case of segmented free-standing micro-TEC, as the pillar height increases, the electrical resistance increases between the top and bottom copper interconnects and the current flowing through the device decreases. At the same time, the increase in height also leads to a decrease in thermal conductance, which in turn causes an increase in the maximum ΔT from 20.1 to 20.45 K as shown in Fig. 7(a).

However, an interesting phenomenon is observed in the case of segmented SimTEC, as the via height increases, both the optimum current and ΔT decreases as shown in Fig. 7(b). As the height of the pillars increases, the volume of glass surrounding the vias also increases. This increasing volume of glass increases the thermal leakage through the substrate (increased thermal losses) and eventually leading to a decrease in device cooling performance. In both cases, the current corresponding to the maximum cooling remains approximately same for varying height, and this current decreases with increasing height due to the increasing electrical resistance of the device. The change in ΔT with increasing height is more pronounced in the case of SimTECs as compared to free-standing micro-TECs. In case of SimTEC, the maximum ΔT is 5.28, 4.2, and 3.62 K for the via heights 50, 75, and 100 μm, respectively. Hence, larger height of vias deteriorates the cooling performance in the case of SimTEC. As shown in Table 5, the cooling capacity for both free-standing micro-TEC pillars and the SimTEC vias decreases with increasing height due to the increase in both electrical and thermal resistances of the device.

3.4 Effect of SimTEC via Pitch

In case of both free-standing micro-TEC pillars and SimTEC vias in glass substrate, the via/pillar height and diameter are kept constant at 100 and 30 μm, respectively. The via/pillar pitch is

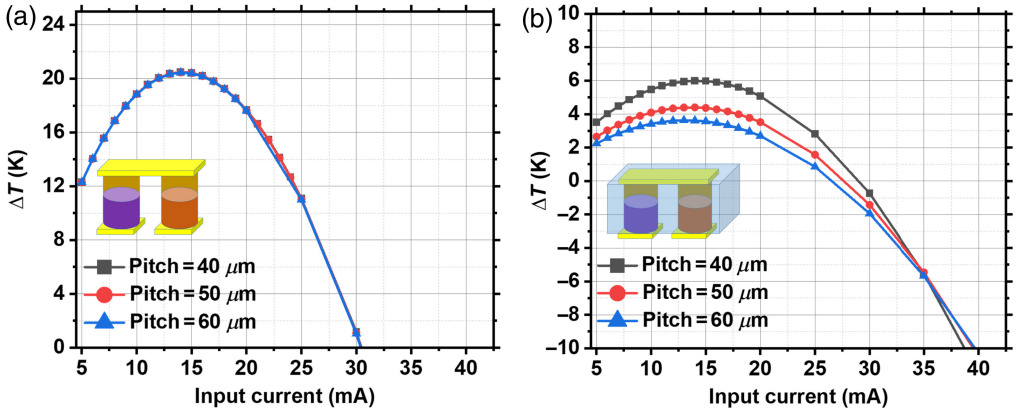

Fig. 8 Graphs showing the change in temperature gradient in the case of (a) free-standing micro-TEC pillars and (b) SimTEC vias when the pitch of the vias/pillars partially filled with copper/thermoelectric material is varied from 40 to 60 μm, when the diameter and height of the vias/pillars are kept constant.

Table 6 Cooling capacity of free-standing micro-TEC pillars and SimTEC vias when $\Delta T = \Delta T_{max}$ for different pillar/via pitches.

	Q_c (mW)	
Pitch (μm)	Free-standing micro-TEC	SimTEC in glass
40	0.002252	0.3415
50	0.002447	0.3785
60	0.002652	0.3898

increased from 40 to 60 μm in SimTEC and free-standing micro-TEC and its effect on the cooling performance is analyzed in each case. In both cases [Fig. 8(a) and 8(b)] as the pitch is increased, the cooling performance of the device is decreased. In the case of free-standing micro-TEC, the small decrease in ΔT can be attributed to the small increase in the device electrical resistance. The decrease of the maximum ΔT in the case of SimTEC is more pronounced as compared to that of the free-standing micro-TEC.

This significant decrease in maximum (ΔT) is because of the increasing glass volume between the vias as the pitch increases, leading to an increasing parallel thermal conductance path between the top and bottom copper interconnects on the glass substrate. The maximum ΔT achieved is 5.99, 4.4, and 3.63 K for 40, 50, and 60 μm pitches, respectively. Interestingly, the current corresponding to the maximum device cooling performance remains the same at ~14 mA in both cases because the via dimensions remain unchanged.[31] The cooling capacity for both the cases (free-standing micro-TEC pillars and SimTEC vias) increase with an increase in the pillar/via pitch mainly due to the decrease in ΔT_{max}, as the current corresponding to maximum cooling remains the same (Table 6).

3.5 Effect of SimTEC Fill Factor

In case of both segmented free-standing micro-TEC pillars and segmented SimTEC in glass substrate, the via/pillar height, diameter, and pitch is fixed as 100, 30, 60 μm, respectively. The volume of the thermoelectric material is increased from 25% to 100% in the vias/pillars. This filling ratio of thermoelectric material in the via/pillar is denoted as fill factor, which is changed from 0.25 (a quarter filled with thermoelectric material) to 1 (fully filled with thermoelectric material). In case of free-standing micro-TEC, as the fill factor of the thermoelectric material increases, the maximum temperature gradient of the device increases by a small proportion as shown in Fig. 9(a). This is due to the increment in the volume of thermoelectric

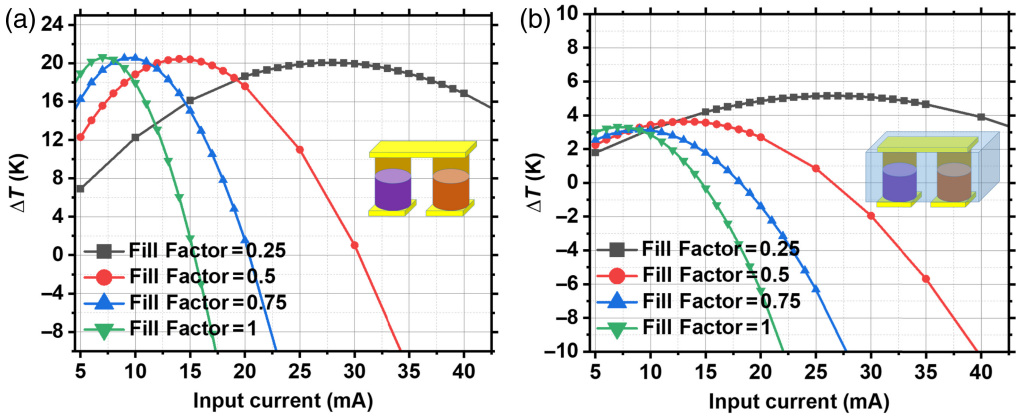

Fig. 9 Graphs showing the change in temperature gradient in case of (a) free-standing micro-TEC pillars and (b) SimTEC vias when the fill factor (filling ratio of thermoelectric material and copper in vias/pillars) is varied from 25% (1/4th of the cylinder filled with thermoelectric material and 3/4th of the cylinder is filled with copper) to 100% (the whole cylinder is filled with thermoelectric material), when the diameter, pitch, and height of the vias/pillars are kept constant.

Table 7 Cooling capacity of Free-standing micro-TEC pillars and SimTEC vias configurations when $\Delta T = \Delta T_{max}$ for different fill factors.

	Q_c (mW)	
Fill factor of TE material	Free-standing micro-TEC	SimTEC in glass
0.25	0.012321	0.7039
0.5	0.002652	0.3898
0.75	0.001088	0.2713
1	0.000504	0.2036

material between the copper interconnects on the top and bottom of the pillars which enhances the contribution of the Peltier effect.

Conversely, in case of SimTEC vias as the volume of the thermoelectric material increases, the maximum ΔT decreases as shown in Fig. 9(b). The reason behind this is change of the primary heat flow path from the thermoelectric material filled vias to glass substrate (as the thermal conductivity of glass substrate is higher than the thermal conductivity of the thermoelectric materials) leading to an increased thermal conductance between the top and bottom copper interconnects. When the fill factor is varied from 0.25 to 1, the maximum ΔT falls from 5.15 to 3.31 K. The decrease in maximum ΔT for SimTEC is more pronounced as compared to the increase in ΔT for the free-standing micro-TEC. The different current values corresponding to the maximum ΔT of the device as the fill factor is increased remains approximately same in the case of SimTEC vias and free-standing micro-TEC pillars. The electrical resistance of the vias/pillars increases with increasing volume of thermoelectric material and decreasing copper volume. This explains the trend of decreasing optimum current value with increasing fill factor. The decreasing cooling capacity of the free-standing micro-TEC pillars and SimTEC vias with increasing fill factor (of thermoelectric material) is accounted due to the increase in electrical and thermal resistance of the device (Table 7).

3.6 Optimization Analysis for SimTEC

Design of experiments (DOE) is an established method to highlight the effect of multiple factors on the response of the resultant parameter.[32] In our case, the independent factors, such as diameter, height, and pitch of the vias in SimTEC and the pillars in free-standing micro-TEC are

Table 8 DOE for the three geometrical factors (diameter, height, and pitch) of the free-standing micro-TEC pillars and SimTEC vias showing their impact on the temperature gradient and cooling power of free-standing micro-TEC and SimTEC device.

Number	Diameter (μm)	Height (μm)	Pitch (μm)	Max (ΔT) free-standing (K)	Q_c free-standing micro-TEC (mW)	Max (ΔT) SimTEC (K)	Q_c SimTEC (mW)
1	30	50	60	20.1067	0.008074462	5.2848	0.697759
2	30	75	80	20.2882	0.005066396	3.6226	0.513925
3	40	50	60	20.0673	0.014681976	7.1296	1.089483
4	40	75	60	20.3092	0.007614643	6.1392	0.793398
5	40	50	80	19.9796	0.018598842	6.2246	1.156967
6	40	75	80	20.2497	0.009387806	4.9708	0.851657
7	30	50	100	19.9685	0.011643759	4.6711	0.717313
8	50	50	100	19.8263	0.037062469	7.0281	1.692721
9	30	100	60	20.4514	0.002651843	3.6294	0.389838
10	50	50	60	20.0467	0.022090723	9.3069	1.421228
11	50	100	60	20.4226	0.007418645	7.9608	0.820746
12	30	100	100	20.3825	0.003538767	2.6737	0.400488
13	50	100	100	20.309	0.011386614	4.8139	1.00867
14	30	75	100	20.2403	0.005896732	3.3898	0.520577
15	40	100	60	20.4336	0.004917396	5.5472	0.624838
16	40	50	100	19.8902	0.022671149	5.9362	1.172181
17	50	50	80	19.9367	0.02985582	7.5244	1.642173
18	50	75	60	20.297	0.011625882	8.5025	1.037028
19	30	100	80	20.4172	0.003089285	2.9448	0.405407
20	40	100	80	20.3882	0.005933945	4.2368	0.67331
21	40	100	100	20.3419	0.006987212	3.7337	0.685747
22	50	75	80	20.2219	0.015031876	6.3777	1.212063
23	50	100	80	20.3664	0.009330016	5.658	0.961647
24	50	75	100	20.1455	0.018691193	5.6683	1.265605
25	30	50	80	20.0382	0.009833355	4.8414	0.710663
26	30	75	60	20.3354	0.004257387	4.2092	0.504128
27	40	75	100	20.1891	0.011226951	4.5552	0.866411

varied and the resulting effect on the variation of maximum temperature gradient across the device is analyzed. The diameter, height, and pitch of the vias/pillars are all varied among three values. The diameter is varied between 30 40, and 50 μm; height is varied between 50, 75, and 100 μm; and the pitch is varied between 60, 80, and 100 μm. In addition, the pitch is varied such that it is twice the diameter values. The resulting maximum temperature gradient and cooling power in this $3 \times 3 \times 3$ factorial design is also tabulated for both cases of SimTEC and free-standing micro-TEC, where the fill factor is kept constant at 0.5 (Table 8).

Figure 10 shows the change in maximum temperature gradient (ΔT) across all three parameters (diameter, height, and pitch); where the trends $(\Delta T/\Delta D)_{P,H}$ observed in the SimTEC is

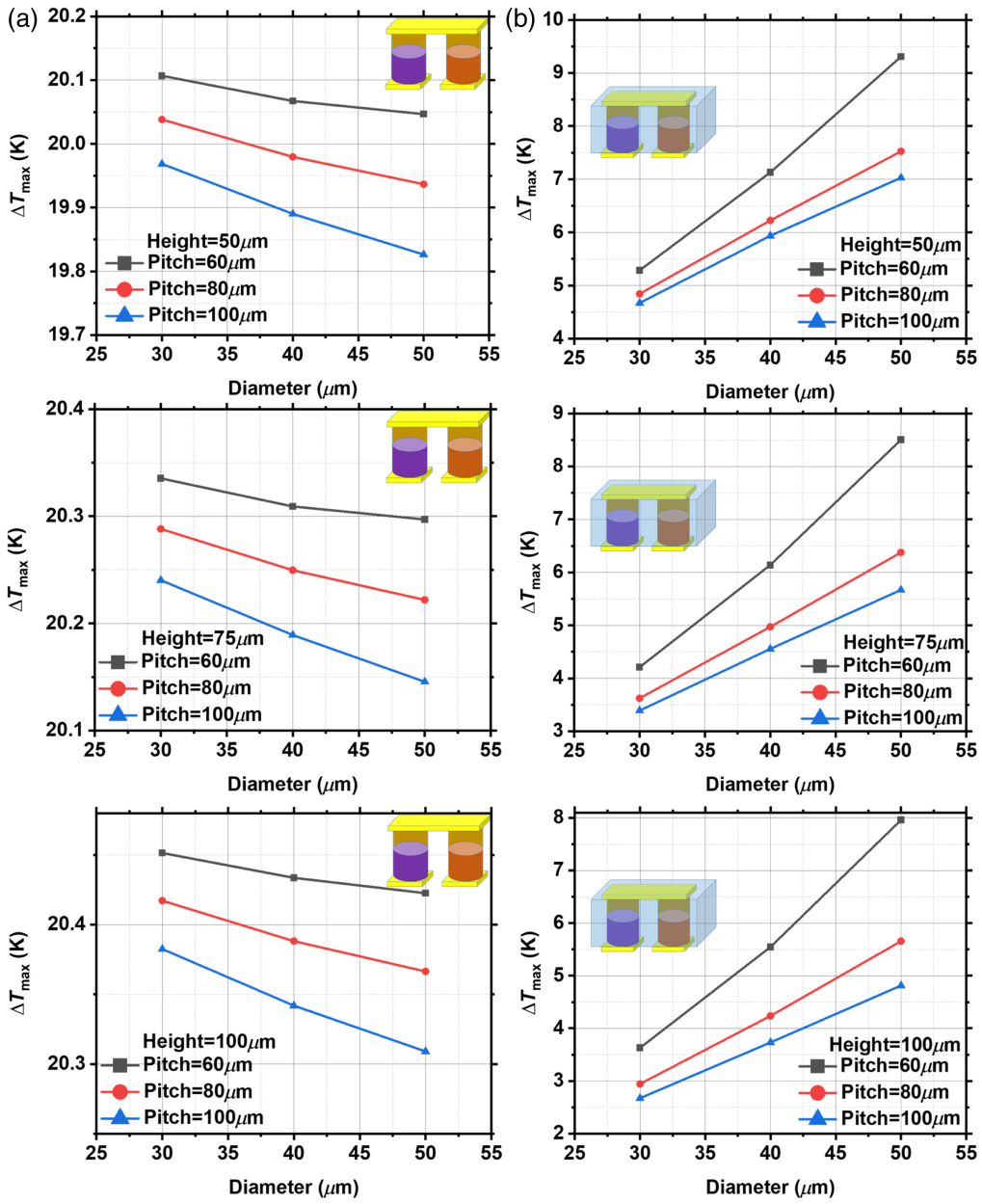

Fig. 10 Graphs showing the change in the maximum temperature gradient of (a) free-standing micro-TEC pillars and (b) SimTEC vias when the diameter, height, and pitch of the vias/pillars are varied simultaneously where the fill factor if the via/pillar is kept constant at 50%.

opposite to that observed in the equivalent free-standing micro-TEC structure. The influence of the geometrical parameters of the pillars in terms of thermal resistance and electrical resistance of the device in turn affects the maximum temperature gradient and cooling power. In addition to this, the thermal losses in the glass substrate impacts the opposing trend of maximum temperature gradient with changes in diameter and height of SimTEC as compared to the free-standing micro-TEC.

Moreover, these thermal losses due to the glass substrate are mainly responsible for the decrease in maximum temperature gradient ($\Delta T = 9.3$ K) for SimTEC as compared to the maximum temperature gradient ($\Delta T = 20.45$ K) for free-standing micro-TEC, amounting to a decrease of ~54%. In case of free-standing micro-TEC, averaging the impact of diameter, height, and pitch of TEC pillars on the change in maximum temperature gradient shows that the order of this impact is height > pitch > diameter. However, for the SimTEC vias, parametric impact on

change in maximum temperature gradient (ΔT) across the TEC follows the order of diameter > height > pitch.

This parameter variation also allows the maximum temperature gradient (ΔT) in SimTEC, which varies from a minimum of 2.67 K to a maximum of 9.3 K, amounting to a total variation of 6.63 K. Although in micro-TEC, it only allows for the variation of a maximum cooling range from 19.82 to 20.45 K (total variation of 0.63 K). Interestingly, this ΔT variation in case of free-standing micro-TEC pillars (19.82 to 20.45 K) leads to a decrease in cooling capacity from 0.037 to 0.002 mW, which then leads to a trade-off between $\Delta T_{\max}$ and Q_c (at $\Delta T_{\max}$). The ΔT variation in case of SimTEC vias (2.67 to 9.3 K) allows for a corresponding increase in cooling capacity from 0.4004 to 1.42 mW.

4 Conclusion

The integration of TEC capabilities in glass substrates through the SimTEC approach provides a highly attractive thermal management solution for next generation highly integrated electronic–photonic packaged systems. It addresses the need for thermal isolation and control between package components, while maintaining a compact form factor. This work has presented a theoretical analysis of the cooling capability of SimTEC and compared its cooling performance to similar sized free-standing micro-TEC device. The glass platform in this design provides structural rigidity and allows the fabrication processes to be relaxed for embedded microscale thermoelectric coolers. As discussed in this work, the disadvantage of the SimTEC approach is that higher thermal conductivity of the glass compared to the thermoelectric materials acts to diminish the overall cooling potential. As a result, the maximum temperature gradient of SimTEC decreases by ~6 times as compared to the maximum temperature gradient of free-standing micro-TEC device, which is discussed in Sec. 3.1. This discrepancy primarily arises due to the thermal losses in the glass substrate.

Notably, the range of variation in maximum ΔT resulting from changes in via parameters (diameter, height, and pitch altered concurrently) in SimTEC is 6.63 K, as compared to a mere 0.63 K in the equivalent free-standing micro-TEC device. This range illustrates that increasing the via diameter, decreasing the via height, and reducing the via pitch enhances the cooling performance in SimTEC, with a peak improvement of $\Delta T = 9.3$ K achieved when the fill-factor ratio of thermoelectric material and copper in the pillar/via is maintained constant at 0.5. Moreover, within the simulated range of via parameters, the thermal tuning capability of SimTEC stands at 18.6 K (2×9.3 K). This allows for both heating and cooling of the top via interconnect and photonic chips through the reversal of input current polarity based on environmental thermal fluctuations.

However, it is important to acknowledge that despite its advantages, the cooling capability of SimTEC remains inferior to that of the free-standing micro-TEC device. As a result, SimTEC is better suited for thermal stabilization rather than specialized cooling applications. Nevertheless, the potential for enhancing SimTEC thermal tuning and cooling efficiency lies in optimizing the performance of the thermoelectric material (zT), which would facilitate a more efficient thermoelectric conversion process and consequently increase the temperature gradient across the top and bottom interconnects of SimTEC vias.

5 Future Work

The next steps for this work are to include the simulation of complete SimTEC devices in the glass interposer underneath the electronic integrated chips (EICs) and photonic integrated chips (PICs) and analyze the active temperature control of the PIC/EIC. The authors also envision that the SimTEC architecture can be expanded to a multilayered glass substrate,[33] where the thin glass substrate layer with SimTEC can be stacked on top of the glass substrate layer with SimTEG. This will enable the heat load pumped out from the hot side of the SimTEC layer to be used as an input by the SimTEG layer[34] for power generation in the package.

Disclosures

There are no conflicts to declare.

Code and Data Availability

Data will be made available on request.

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Parnika Gupta is currently pursuing her PhD, which focuses on the design, assembly, and testing of glass interposers for co-packaged photonic integrated circuits and electronic integrated circuits under the supervision of Prof. Peter O'Brien at Tyndall National Institute. The aim for her research is to generate design rules for effective thermal management of co-packaged electronic and photonic chips on glass interposer. She received her MS degree from the National Taiwan University of Science and Technology in 2019 under the supervision of Prof. San Liang Lee, where she worked on the design, fabrication, and characterization of silicon micromirrors for optical coupling between laser and photonic chips. Prior to this, she completed her bachelor's degree in electronics and communication engineering from MDU, Rohtak, in 2016. Her current research interests include thermal management in advanced packages, high-speed package interconnects, thermoelectric devices, advanced packaging technologies, and optical interconnects.

Amit Tanwar is a research student (PhD) in the AEM group and his research mainly focuses on the development of thermoelectric materials using the electrodeposition method and fabrication of microthermoelectric generator for wearable applications. He received his bachelor's and master's degrees in electronics in India.

Xiuyun He is a senior mechanical design engineer in the Photonic Packaging Group, Tyndall National Institute, Ireland. She earned her bachelor's degree of industrial design (overall ranking no. 1) and her master's degree of engineering from the Northeastern University, China, in July 2005 and March 2008, respectively. In September 2016, she was awarded her PhD in mechanical engineering at Heriot-Watt University, United Kingdom.

Kamil Gradkowski earned his MScEng degree in applied physics from Warsaw Institute of Technology, Warsaw, Poland, in 2006, and his PhD in applied physics from the Cork Institute of Technology, Cork, Ireland, in 2010. He is currently a packaging engineer in the Photonics Packaging Group, Tyndall National Institute, Cork, Ireland.

Kafil M. Razeeb is a principal scientist, leading the Advanced Energy Materials Group at Tyndall National Institute of the University College Cork. He received his PhD from the University of Limerick in 2003. He has authored or co-authored 10 book chapters and more than 120 peer-reviewed journal articles and conference presentations. He is a senior member of IEEE and a chartered physicist and a member of Institute of Physics.

Padraic E. Morrissey is a technology manager of the PIXAPP Pilot Line for Photonic Packaging and Assembly. His research interests focus on the development of standardized photonic packaging technologies leading to new optical and electrical packaging schemes for Si and InP-based photonic systems. He has a demonstrated history of leading and managing photonic technology research across large, multipartner EU projects and industrial engagements. He received his PhD in physics from the Tyndall National Institute in 2014.

Peter O'Brien is a director of the PIXAPP Photonics Packaging Pilot Line and head of the Photonics Packaging Group at the Tyndall Institute. He is also a lead partner in the InP Pilot Line (InPulse), SiN-PIC Pilot Line (PIX4LIFE), and is a member of ACTPHAST TCT team, JEPPIX, and ePIXfab steering committees. His group develops photonic microsystems for high-speed fiber-optic communication, medical devices, and sensing applications.