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Low-power, low-pressure reactive-ion etching process for silicon etching with vertical and smooth walls for mechanobiology application

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Abstract. We report our findings in developing a low-power etching recipe using a newly acquired reactive-ion etching (RIE) tool (RIE-10NR, Samco, Japan), with the aim of achieving smooth and vertical sidewalls in micropatterned silicon substrate. We used a combination of CF_4, SF_6, and O_2 gases, which at low power (30 W) and low pressure (2 Pa) allowed for vertical silicon etching (aspect ratio ~2). We used photoresist and silicon oxide as the etching masks. As it is a continuous etching process, scalloping effects were not present, which is contrary to the process done with an inductively coupled plasma-based "Bosch" approach. We also show a successful use of these microstructures as master mold in soft-lithographic techniques for producing devices in elastomeric materials that have applications in mechanobiology. To the best of our knowledge, the recipe we present here has the lowest combination of power and pressure for etching silicon with vertical profile using a standard, parallel plates RIE tool. [DOI: 10.1117/1.JMM.16.3.034501]

Keywords: reactive-ion etching; silicon etching; pattern transfer.

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1 Introduction

Structuring of silicon using plasma etching is one of the most extensively used techniques for the fabrication of silicon-based devices and molds mostly so when high-dimensional fidelity and verticality are required.[1–4] Key parameters in optimizing an etching step are comprehensive for but not limited to selectivity with respect to the masking material, lateral erosion, and surface finishing. There are alternative approaches for the structuring of silicon, such as alkaline wet etching[5–7] or the more recently introduced metal-assisted chemical etching (MACE).[8] Anisotropic wet etching exploits differential etching rates of silicon in different crystalline directions, therefore, its applicability is difficult for complex or arbitrarily designed geometries; on the other hand, MACE, while compatible with complex geometries, requires a metal deposition step and uses an hydrofluoric acid-based chemical bath, which nowadays is regarded as a safety hazard and is recommended to be avoided where possible. Overall, plasma etching is still the preferred choice where a plane geometry has to be transferred into the silicon substrate with vertical walls. An inductively coupled plasma (ICP) tool uses the "Bosch" process to achieve high aspect ratio structures but may encounter limitations in the form of undesired effects, such as scalloping (sidewall undulation inherent in the Bosch process) and aspect ratio-dependent etching.[9,10] A simpler and relatively inexpensive tool using reactive-ion etching (RIE) has limitations in producing deep vertical silicon structures and is more often used for isotropic etching.

At Mechanobiology Institute (National University of Singapore), our "microfabrication core" facility has recently acquired a planar plates RIE tool (RIE-10NR, Samco, Japan, see Fig. 1) for the production of microstructured silicon molds. These molds are used to replicate the structures on biocompatible materials (such as polydimethylsiloxane, commonly known as PDMS) using soft lithography, e.g., cast molding. These biocompatible devices can be applied as protein stamping tools,[11] microfluidic/microoptical devices,[12,13] and quite often used as substrates for biological studies. One such application is the use of micro-PDMS pillars as force-sensing tools in traction force microscopy.[14]

Generally, when the required height of silicon structures (or molds) is tens of micrometers, a surface modulation induced by scallops in the range of hundreds of nanometers can be neglected. In such a scenario, an ICP-based Bosch process will be ideal. However, in most of our applications, we deal with 1- to 2-μm diameter pillars where hundreds of nanometers of scallops would have undesired effects on our experiments, thus providing the motivation for this work.

In this paper, we report our findings in developing an RIE-based fabrication process to produce silicon microstructures with good surface finishing. Our process used a combination of CF_4, SF_6, and O_2 gases, which at low power (30 W) and low pressure (2 Pa) allowed for vertical etching of silicon with an aspect ratio up to ~2. As it was a continuous etching process, scalloping was not present. During the course of this study, we explored the etching selectivity of different materials with respect to silicon and developed a second recipe to pattern silicon oxide that had the highest selectivity. Here, we discuss both the etching recipes, their limitations, and suitability for mechanobiology applications.

2 Materials and Methods

Standard, prime grade, ⟨100⟩ silicon wafers both with and without a thermally grown 300-nm thick silicon oxide layer were used. For the lithographic steps, both positive tone (AZ5214E, Clariant Corporation, Switzerland) and negative

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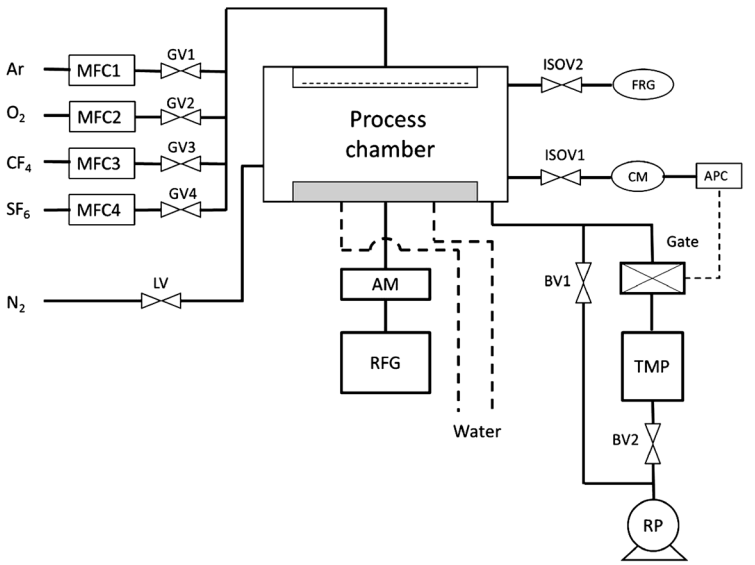


COMPONENTS LIST	
MFC1-4	Mass flow controllers
GV1-4	Gas inlet valves
LV	Leak valve
BV1-2	Evacuation valves
ISOV1-2	Isolation valves
CM	Capacitance manometer
FRG	Full range gauge
TMP	Compound turbo molecular pump
RP	Rotary pump
AM	Automatic impedance matching unit
RFG	Radio frequency generator
APC	Automatic pressure controller

Fig. 1 Block diagram of the RIE-10NR used in this work. The RIE is a standard, parallel plates tool; its process chamber is an aluminum cylinder of 340-mm diameter and 170-mm height, whereas both upper and lower electrodes have a diameter of 240 mm. Four gas lines are installed for O_2, Ar, CF_4, and SF_6. The radio frequency generator can provide a maximum power of 500 W.

tone (SU-8, Microchem Corporation) photoresists were exposed using an MJB4 mask aligner (SussTech, Germany). The mask aligner was equipped with an Hg-Xe UV lamp (500 W). The height of the structures fabricated and the thickness of the photomask layer was measured with a Dektat XT stylus profiler (Bruker, Germany). Verticality and surface finishing of the sidewalls were observed and estimated with a JSM-6010LV scanning electron microscope (SEM, Jeol, Japan).

2.1 *Etching Recipes*

Two recipes were developed. The first recipe (recipe A) was developed to produce vertical and smooth sidewalls on silicon. Masks used were photoresists (AZ5214E and SU-8) and silicon oxide. The second recipe (recipe B) was developed to pattern the oxide layer used as a mask for silicon etching. AZ5214E was used as a mask for silicon oxide etching using recipe B. Table 1 summarizes parameters for both the recipes.

2.2 *Samples Preparation*

2.2.1 *AZ5214E mask*

Silicon wafer was dehydrated on a hot plate at 200°C for 30 min. After 5 min of cooling, it was primed with hexamethyldisilazane (HMDS) for promoting better adhesion with the photoresist. Then, AZ5214E was spin coated at 4000 rpm for 45 s and baked at 100°C for 100 s; after 1 min of cooling, the wafer was ready for exposure.

Exposure was done on the mask aligner for 6 s at a lamp intensity of 24 mW/cm^2 measured at 365-nm wavelength. Development was done with 3 min immersion in AZ400K developer diluted at 1:4 in de-ionized (DI) water. After rinsing in DI water and blow-drying with nitrogen, the wafer was ready for silicon etching. The thickness of the photoresist was measured using the stylus profiler and was found to be $\sim 1\ \mu m$.

Table 1 Optimized parameters for the two recipes.

	Recipe A	Recipe B
Gas flow (sccm): $CF_4/SF_6/O_2$	40/10/10	40/0/4
Power (W)	30	150
Pressure (Pa)	2	15

2.2.2 *SU-8 mask*

Silicon wafer was dehydrated on a hot plate at 200°C for 30 min. After 5 min of cooling, negative-tone resist SU-8 3005 was spin coated at 3000 rpm. Prebaking was carried at 65°C for 1 min and 95°C for 2 min. After 1 min of cooling, the wafer was ready for exposure.

Exposure was done on the mask aligner for 4 s at a lamp intensity of 20 mW/cm^2 measured at 365-nm wavelength. i-line filters were used for the exposure. Postexposure bake was done at 65°C for 1 min and 95°C for 2 min followed by development in SU-8 developer for 1 min. After rinsing in isopropyl alcohol (IPA) and drying with nitrogen, the wafer was ready for silicon etching. The thickness of the resist was measured using the stylus profiler and was found to be $\sim 5\ \mu m$.

2.2.3 *Silicon oxide mask*

Silicon wafer with a 300-nm thick thermal oxide layer was dehydrated on a hot plate at 200°C for 30 min. After 5 min of cooling, it was primed with HMDS for promoting better adhesion with the photoresist. AZ5214E was then spin coated at 4000 rpm for 45 s and baked at 100°C for 100 s. After 1 min of cooling, the wafer was ready for exposure. Exposure was done on the mask aligner for 6 s at a lamp intensity of 24 mW/cm^2 measured at 365-nm wavelength.

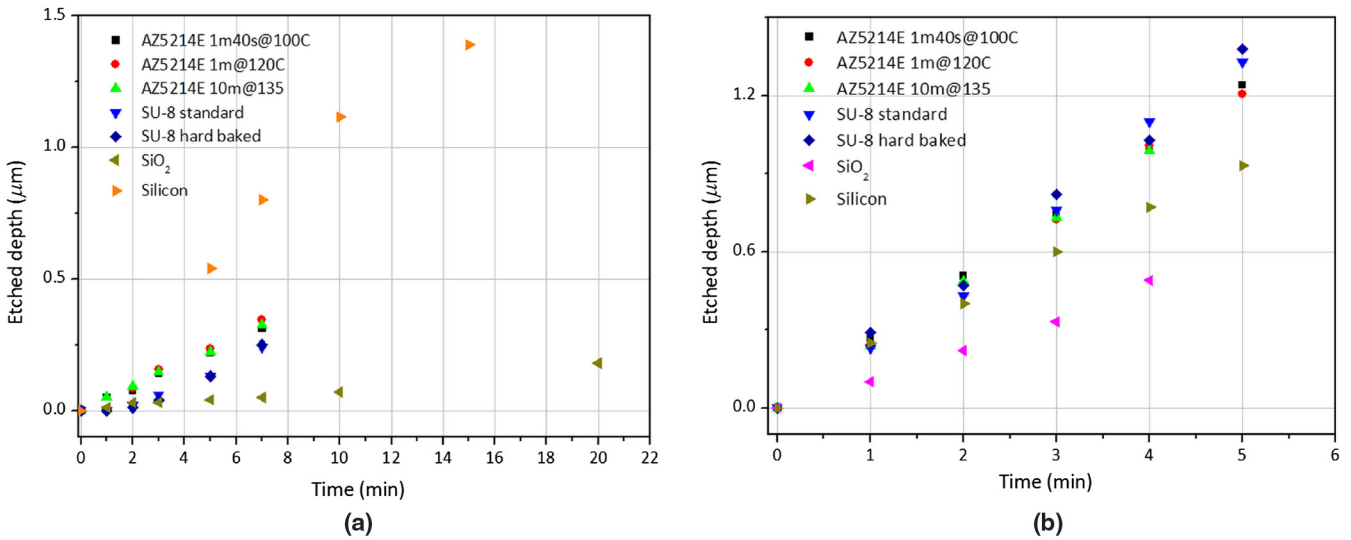


Fig. 2 (a) Etching depth in different materials (as indicated in the legend and described in the text), measured after recipe A was applied for the given times; (b) etching depth in different materials (as indicated in the legend and described in the text), measured after recipe B was applied for the given times.

Oxide was etched for 3 min and 30 s using recipe B (see Table 1). After oxide etching, residual photoresist was removed in an acetone bath with ultrasound applied. The wafer was then rinsed in IPA and dried with a nitrogen gun and was ready for silicon etching using recipe A (see Table 1).

2.3 *Etching Rate Measurement*

Etching rates for all the materials used were measured with the procedure as described below

i. Silicon: Silicon wafer was patterned with AZ5214E resist and diced into small pieces. Five and six such pieces, respectively, were placed in the chamber and etched for different times using recipes A and B. Remaining photoresist was removed in an acetone bath with ultrasound applied. The depth of etching at each controlled time was measured using the stylus profiler.

ii. Silicon oxide: Silicon wafer with thermal oxide layer was patterned with AZ5214E resist and diced into small pieces. Five and six such pieces, respectively, were placed in the chamber and etched for different times using recipes A and B. Remaining photoresist was removed in an acetone bath with ultrasound applied. The depth of etching at each controlled time was measured using the stylus profiler.

iii. AZ5214E with different baking conditions: Silicon wafers coated with AZ5214E were baked at different temperatures and times (as discussed in Sec. 3) and diced into small pieces. Five and six such pieces from each wafer, respectively, were placed in the chamber and etched for different times using recipes A and B. The depth of etching at each controlled time was measured using the stylus profiler.

iv. SU-8: Silicon wafers were coated with SU-8 resist and prebaked with standard conditions (65°C for 1 min and 95°C for 2 min). The wafers were then flood exposed for 5 s at 20 mW/cm^2 measured at 365 nm (with i-line filters in the mask aligner) and postbaked at different temperatures and times (as discussed in Sec. 3). Each wafer was diced into small pieces. Five and six such pieces from each wafer, respectively, were placed in the chamber and etched using recipes A and B. The depth of etching at each controlled time was measured using the stylus profile.

All the wafers were diced into 1 × 1 cm^2 pieces. The etching times used were 1, 2, 3, 5, 7, and 20 min for recipe A and 1, 2, 3, 4, and 5 min for recipe B.

The test features consisted of gratings (line width of 3 and 4 μm with varying gaps of 3, 5, or 10 μm) and square openings (3-μm side and 3-μm gap) for all samples. Additionally, we used dots and holes (both with 2-μm diameter and 2-μm gap) for silicon oxide samples. The performance of both the recipes was also tested on full 4″ wafers, the result of which did not vary from that of the smaller samples.

2.4 *Polydimethylsiloxane Casting*

For casting of PDMS, selected silicon mold was coated with an antisticking layer of octadecyl perfluoro silane through

Table 2 Baking conditions under test for AZ5214E and SU-8 resists.

AZ5214E	SU-8
1. 100°C for 1 min 40 s (optimal prebake)	1. No postdevelopment hard bake
2. 120°C for 1 min (prebake)	2. Postdevelopment hard bake at 120°C for 10 min
3. Optimal prebake + postlithography hard bake at 135°C for 10 min	

Table 3 Summary of etching rates in nm/min at different conditions and the subsequent etching ratio achieved.

Material		Recipe A	Recipe B
AZ5214	1 min 40 s at 100°C	44	250
	1 min at 120°C	49	267
	10 min at 135°C	46	245
SU-8	Standard	34	262
	Hardbake for 10 min at 120°C	35	267
SiO_2		10	110
Si		110	190
Etching rates ratio			
AZ/SiO_2		4.4	2.3
AZ/Si		0.4	1.3
$SU\text{-}8/SiO_2$		3.4	2.4
SU-8/Si		0.31	1.1
Si/SiO_2		11	2.1

vapor exposure for 2 h.[15] PDMS base resin was mixed with its reticulating agent in a 10:1 ratio and was carefully outgassed in a vacuum jar before pouring onto the mold. To help the filling of the cavities, further outgassing was applied before curing the mixture at 70°C for 1 h on a hot plate. After curing, the PDMS films were carefully peeled off and diced into small pieces to be imaged in the SEM.

3 Results and Discussion

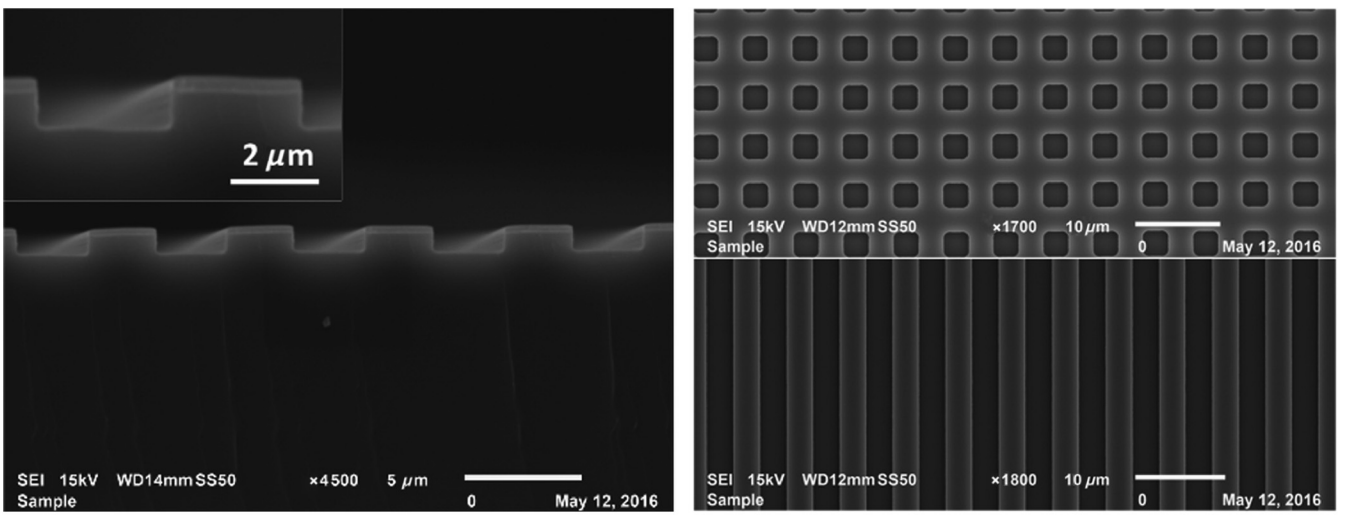
3.1 *Etching Rates and Selectivity*

The etching rate on bare silicon and silicon oxide-coated wafers was evaluated as mentioned in Sec. 2. Both kinds of substrates (silicon and silicon oxide) were coated with the resist mask and were patterned with a step of lithography. The cleared areas were etched and measured at multiple etching times. These data were plotted to get the etching depth versus time curve, the slope of which gave the average etching rate (see Fig. 2).

In the case of photoresists, the possibility of its thermal history playing a role on the measured etching rate was also taken into account. To this task, different pre- and postbaking conditions were tested as summarized in Table 2.

For the AZ5214E photoresist, condition 1 (see Table 2) was found to be optimal, whereas condition 2, although allowed for lithography, had an adverse effect on the resolution of minimum feature size. For condition 3, the effect of an added hard-baking step after the lithography was explored, whereas the prebaking conditions used for lithography were optimal. The AZ5214E resist is shown to have a glass transition temperature above 180°C[16] but started to soften at around 130°C; therefore, 135°C was selected as the temperature for this hard-baking step. At this temperature, the patterned shape was observed to uphold its shape without any noticeable deformation.

Similar logic was used in case of SU-8. The two conditions used were no hard bake and hard bake for 10 min at 120°C (see Table 2). As can be seen from the results reported in graphs [see Figs. 2(a) and 2(b)] and Table 3, different baking conditions were found to have no effect on the etching rate values both for recipes A and B. For recipe A, SU-8 was found to have similar etching rate to that of AZ5214E. Similar etching rates in turn means similar selectivity with respect to silicon, however SU-8 can be coated with a higher layer thickness vis-a-vis AZ5214E resist, and it may then be argued as a preferred choice for masking. As such, SU-8 will



(a) (b)

Fig. 3 (a) SEM picture of silicon grating etched to a depth of 0.7 μm using 0.6-μm thick AZ5214E as a mask. Residual photoresist (~0.3-μm thick) is visible on top of the lines (recipe A); (b) top view of SEM images of a square array and a grating: the clean surface of silicon left after the etching is appreciable, where no micromasking or texturing is noticeable.

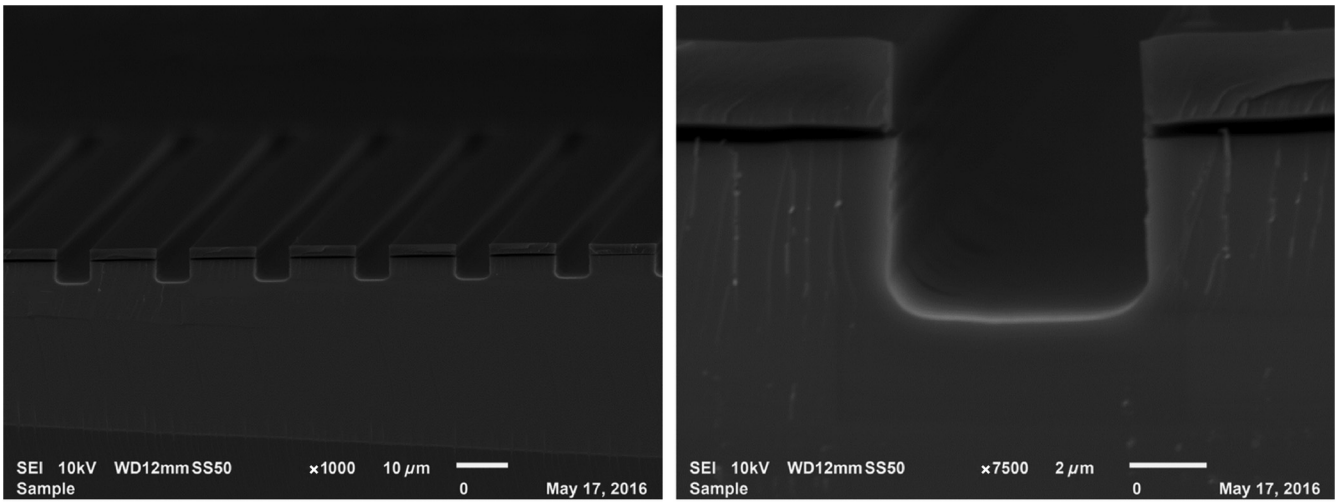


Fig. 4 (a) SEM picture of a grating etched in silicon to a depth of ~4.7 μm using 4.5-μm thick SU-8. Residual 2.3-μm thick resist is visible on top of the lines; (b) close-up view of the etching shown in (a).

hold an advantage, but a thicker SU-8 layer will have an adverse effect on the achievable feature resolution in the lithographic step. For instance, aspect ratios in excess of 3 are challenging in SU-8 when the feature size is in the range of a few micrometers. This consideration limits the advantage of SU-8 as a mask material for our intended application.

As for silicon and silicon oxide, the observed etching rate were, respectively, 190 and 110 nm/min for recipe B and 110 and 10 nm/min for recipe A, as also shown in Table 3. Considering highest selectivity with respect to silicon as our criteria for the mask selection, we clearly see that silicon oxide is the best mask for our process when using recipe A for silicon etching.

3.2 *Silicon Etching with Photoresist Mask*

The performances of recipe A in terms of verticality and surface finishing were at first tested using photoresists as the mask. Figure 3 shows an example of the kind of results achieved when using AZ5214E. In Fig. 3(a), the resulting profile after 7 min of etching is shown ~0.7-μm deep trenches were produced (grating of 3-μm lines with 3-μm gap), with vertical walls as is clearly visible from the SEM picture; in the inset of Fig. 3(a), a closeup of the walls is shown, where the absence of any scalloping is noticeable, and also the remaining layer of the AZ photoresist mask is still visible. Figure 3(b) shows a top view of the same gratings and a square array etched in the same conditions. It is interesting to notice how the silicon surface after the etching step is clean and flat, with no visible texturing or micromasking effects.

The same quality of structures and verticality of the walls was observed when using SU-8 as the masking material, as can be observed in the SEM pictures shown in Fig. 3. Silicon trenches of different width and gap were etched for 40 min at a depth of about 4.2 μm; Fig. 4(a) shows a cross-sectional view of 4-μm wide trenches with a gap of 10 μm, whereas in Fig. 4(b), a closer view is shown where the overall verticality and smoothness of the walls can be observed. The SU-8 mask was initially 3.5-μm thick; after etching, the remaining ~2.3-μm layers are still visible on top of the silicon structures.

These tests were performed using photoresist as the masking material. It was observed in the previous sections that the best choice in terms of selectivity with respect to silicon with recipe A was silicon oxide as the mask. But, the very low etching rate of silicon oxide with recipe A makes it unsuitable for its patterning; hence, recipe B was developed.

3.3 *Silicon Oxide Etching*

In Fig. 5, the result of the oxide etching with recipe B is shown; AZ5214E was coated with a thickness of 1.5 μm and patterned with a hexagonal array of holes of 2-μm diameter and 2-μm gap. After 200 s of etching, the 300-nm oxide layer was removed from the exposed areas and about 0.6 μm of the resist was still left. The slope of the resist walls, generated during the UV lithography step, is clearly noticeable and is apparently reproduced onto the silicon oxide layer.

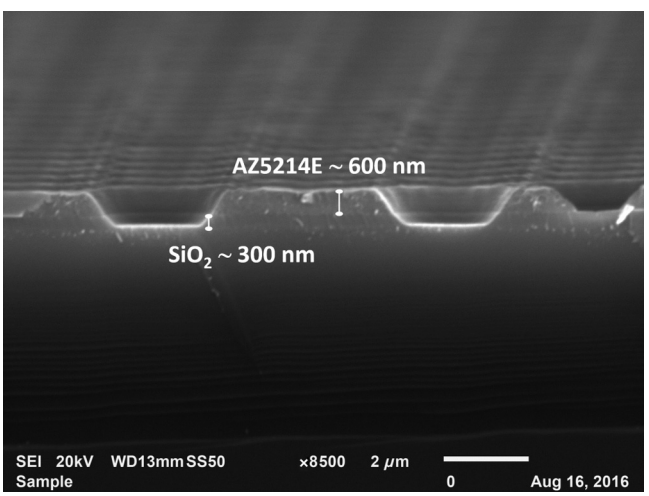
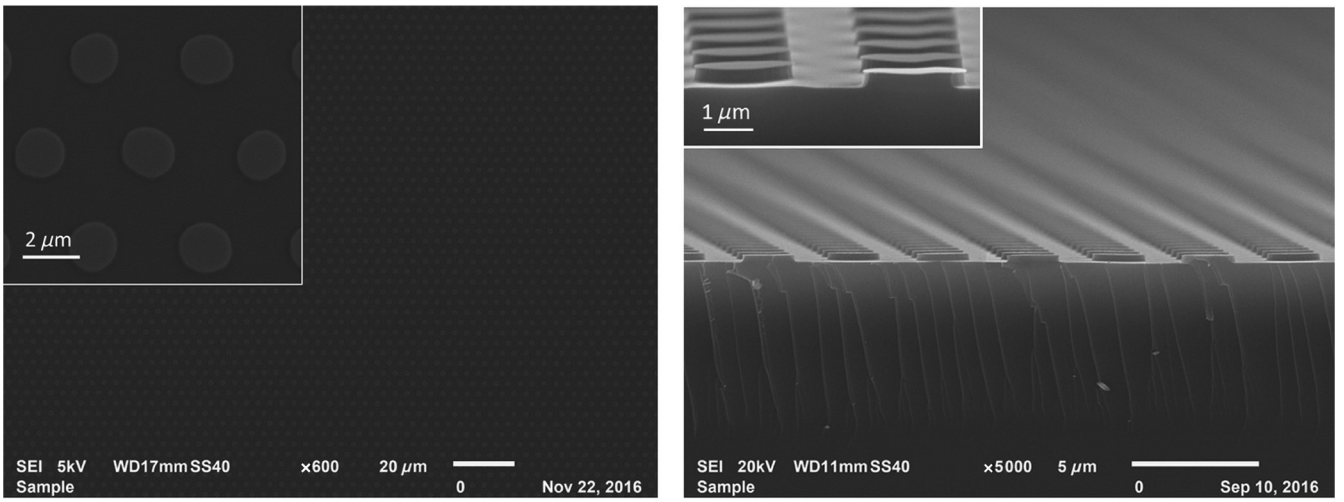


Fig. 5 SiO_2 mask etched for 3 min using recipe B; the residual AZ5214E resist is still visible on the top.



(a) (b)

Fig. 6 (a) SEM picture of the Cr dots produced by liftoff. (b) SEM picture of the oxide layer etched using the Cr mask; in the close-up view, the vertical profile of the oxide structures is more clearly shown.

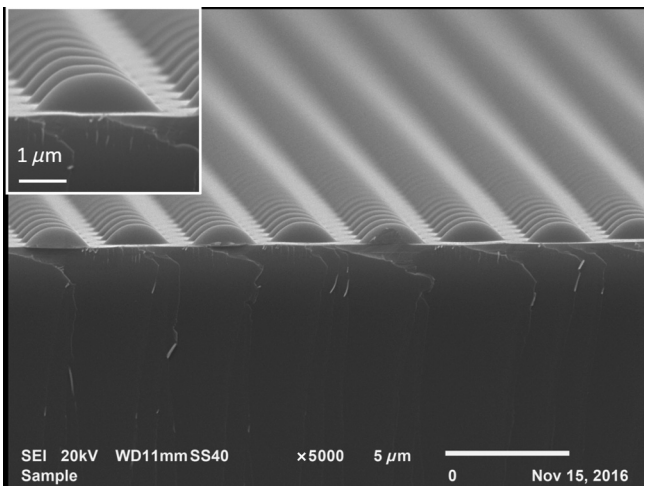


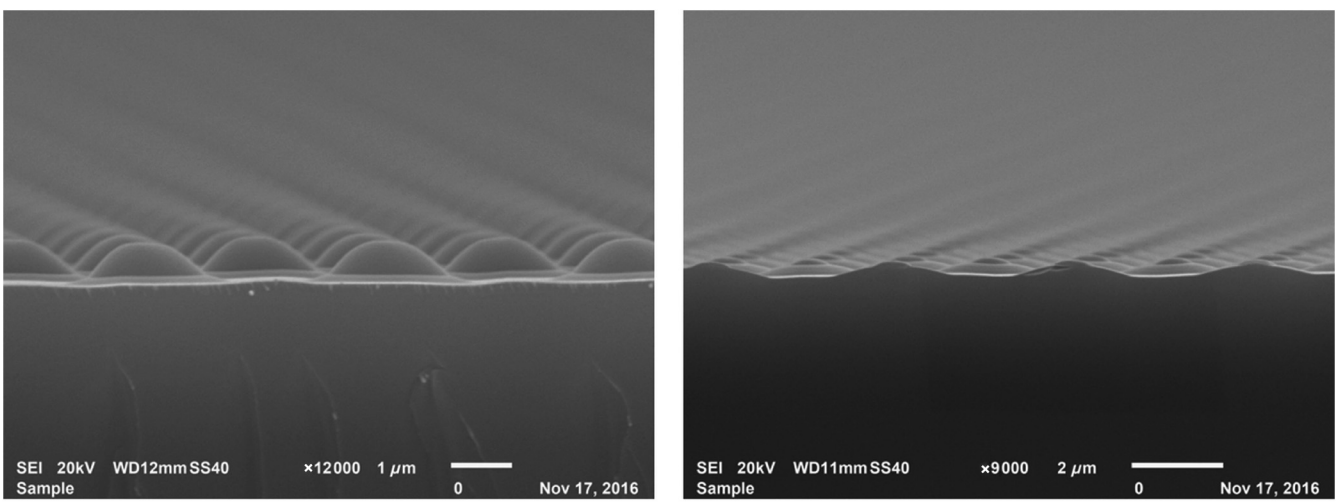
Fig. 7 AZ5214E structures after thermal reflow at 140°C for 10 min.

This consistent transfer of the resist pattern into the oxide layer was further investigated by varying the profile of the mask in two different ways.

In the first approach, an array of Cr dots, 2 μm in diameter and with a 2-μm gap, with a hexagonal array arrangement was produced by means of lift-off [see Fig. 6(a)]. The Cr layer of 40-nm thickness was then used as the mask for etching silicon oxide using recipe B as shown in Fig. 6(b); the resulting etched oxide presented a clear vertical profile. Because of the extremely high-etching resistance of the metal mask, a very low under etching was observed in the oxide underneath.

In the second approach, a curved-shaped mask was produced by thermal reflow of photoresist.[17] A hexagonal array of dots (2-μm diameter and 2-μm gap) patterned in AZ5214E resist with a thickness of 1 μm was reflowed at 140°C for 10 min giving the rounded profiles as shown in Fig. 7.

The oxide was then etched with recipe B using this mask, resulting in the curved lens-like shape as shown in Fig. 8.



(a) (b)

Fig. 8 (a) Silicon oxide etched for 90 s with recipe B with a mask of AZ5214E reflowed curved features; most of the resist is still visible on top of the shallow oxide structures. (b) Recipe B etching applied for 180 s, the silicon oxide etching clearly shows the same lens-like shape as the original AZ5214E mask but with a reduced aspect ratio. A thin residual of the mask is still visible on top of the lenses.

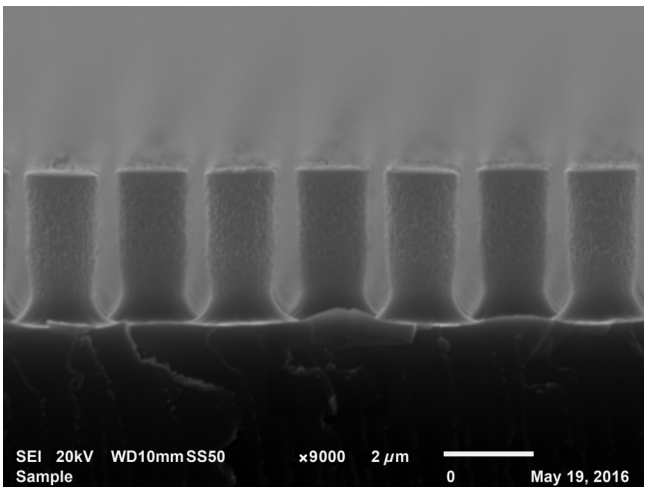


Fig. 9 SEM picture of silicon pillars etched to a depth of ~3.3 μm using 300-nm thick oxide mask. A thin residual oxide is still visible on the top of each pillar.

The aspect ratio of the obtained oxide lens was obviously lower than that in the original resist mask as expected given the etching rates ratio.

3.4 *Silicon Etching with Oxide Mask*

The oxide pattern produced (see Fig. 5) was used as a mask for silicon etching. Pillars thus produced are shown in Fig. 9. These pillars of ~3.3-μm heights were obtained after 30 min of etching; a thin residual of oxide mask is still visible on top. The resulting diameter of the pillars is lower than that of the designed pillars (2 μm) due to the erosion of the mask, which is thinner at the edges. With an estimated diameter of 1.7 μm and height of ~3.3 μm, the achieved aspect ratio is ~2. The surface quality of the pillars is not as good as observed when photoresist was used as a mask (see Figs. 3 and 4). However, this texturing in the range of tens of nanometers is within the tolerance value for the mechanobiology applications.

3.5 *Application for Mechanobiology*

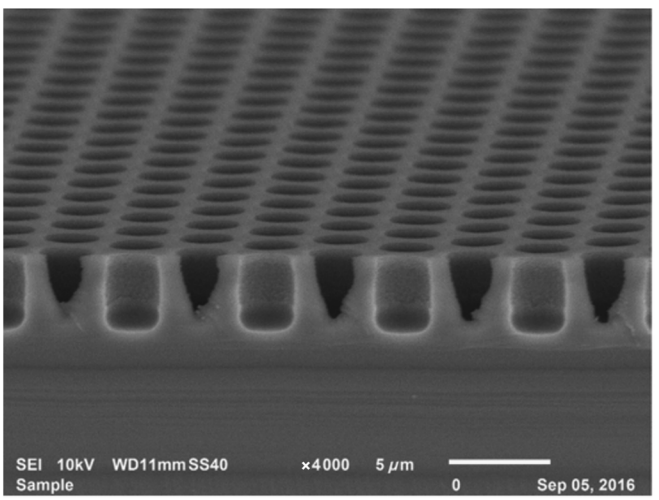
As an application of the presented process, PDMS cast molding of micropillars for traction force microscopy on cells is demonstrated. A silicon mold with 2-μm diameter holes in a close compact array with a gap of 2 μm and depth of 3 μm was fabricated using recipe A with oxide as a mask. The mold, of which an SEM image is shown in Fig. 10(a), was coated with perfluoro silane as an antisticking coating, following the procedure described in Ref. 15. PDMS mixed in ratio 10:1 with its reticulation agent was poured onto the mold and degassed in a vacuum jar for 30 min, to get rid of the air trapped in the holes and let the liquid PDMS fill the cavities. After curing for 1 h at 80°C, the hardened PDMS was carefully peeled off, and an SEM picture of the obtained micropillars is shown in Fig. 10(b).

4 Conclusions

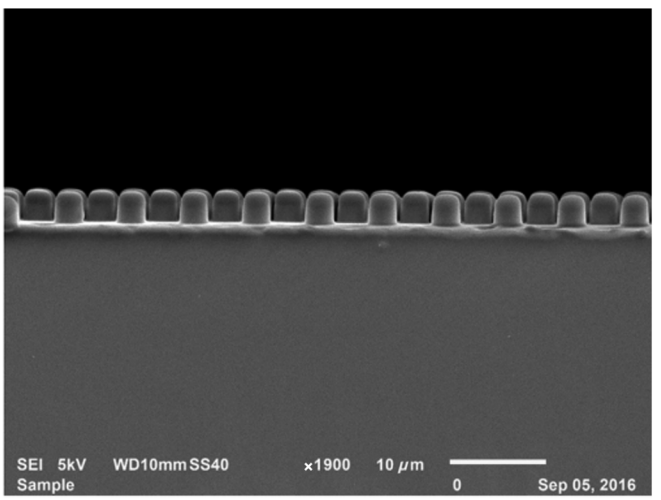
In this paper, we demonstrated a process to fabricate structures in silicon with vertical sidewalls, using a low-power, low-pressure recipe in an RIE tool, which used silicon oxide as the mask material. Surface finishing of the silicon structures was not affected by scalloping, as is usually present in the ICP-based Bosch process. We managed to achieve a smooth finishing for grating and similar linear structures with the use of a polymeric mask (e.g., square or rectangular wells).

To fully exploit the best selectivity for the mask/substrate combination, a secondary silicon oxide etching recipe was developed. During this step, the oxide mask was produced with an induced slope of the walls, which appeared to reproduce the geometry of the resist upon UV lithography. This behavior has been confirmed with the use of a metal mask that gave vertical oxide structures, and a lens-like polymer produced via thermal reflow that gave a similar lens-like oxide structure. The lower aspect ratio in the latter case was due to the difference in etching rates from polymer to oxide.

Finally, we have shown an application of the presented processes in the production of micropillars made out of



(a)



(b)

Fig. 10 (a) Silicon mold and (b) replicated PDMS pillars.

PDMS; a type of structured substrate often used in traction force microscopy. The PDMS pillars formed appear to have a smooth surface at a level adequate for their final application in mechanobiology.

This process was primarily developed for mechanobiology applications but may find other use, such as for producing nanoimprint lithography molds, where either the surface finish for vertical walls of nanostructures is critical or the positively sloped mold profile is seen helpful in the demolding step.

Acknowledgments

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