

Implementing commercial inverse design tools for compact, phase-encoded, plasmonic digital logic devices

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Abstract. Numerical simulations have become an essential design tool in the field of photonics, especially for nanophotonics. In particular, 3D finite-difference-time-domain (FDTD) simulations are popular for their powerful design capabilities. Increasingly, researchers are developing or using inverse design tools to improve device footprints and performance. These tools often make use of 3D FDTD simulations and the adjoint optimization method. We implement a commercial inverse design tool with these features for several plasmonic devices that push the boundaries of the tool. We design a logic gate with complex design requirements as well as a y-splitter and waveguide crossing. With minimal code changes, we implement a design that incorporates phase-encoded inputs in a dielectric-loaded surface plasmon polariton waveguide. The complexity of the requirements in conjunction with limitations in the inverse design tool force us to make concessions regarding the density of encoding and to use on-off keying to encode the outputs. We compare the performance of the inverse-designed devices to conventionally designed devices with the same operational behavior. Finally, we discuss the limitations of the inverse design tools for realizing complex device designs and comment on what is possible at present and where improvements can be made. © The Authors. Published by SPIE under a Creative Commons Attribution 4.0 International License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI. [DOI: [10.1117/1.JNP.17.016011](https://doi.org/10.1117/1.JNP.17.016011)]

Keywords: nanophotonics; inverse design; finite-difference time-domain simulation; plasmonics; surface plasmon polaritons; digital logic; optical logic; phase-shift keying.

Paper 22125G received Nov. 22, 2022; accepted for publication Feb. 23, 2023; published online Mar. 20, 2023.

1 Introduction

Over the past two decades, using simulation design tools has become the standard approach for new nanophotonic designs. In particular, 3D finite-difference time-domain (FDTD) simulations are very popular. These tools allow for fast iteration and robust exploration of the design space at a low cost.¹⁻⁵ Furthermore, they tend to be relatively easy to use and accurate, making them accessible to photonics researchers and designers with a wide variety of backgrounds. Therefore, 3D FDTD simulation tools are a valuable first step for design and a strong theoretical complement to experimental results.

More recently, inverse design tools have begun to emerge as a method of finding optimized designs quickly without needing to explore the entire design space.⁶⁻¹¹ These tools allow researchers to define a figure of merit (FOM) and use the tool to find optimized, nonintuitive designs, which maximize or minimize that figure. They often implement the adjoint method in conjunction with FDTD or FDFD (finite-difference frequency-domain) simulations to perform optimizations. The FDTD software we use is Lumerical, one of the most popular commercial FDTD software packages that includes a packaged inverse design tool which leverages an integration with Python code.¹² This tool is designed to be easy-to-use and robust and is therefore suitable for researchers who may not be able to write their own inverse-design algorithm, which can be quite difficult to implement. Despite this promise, these commercial inverse design tools have some limitations when it comes to certain complex design considerations.

Inverse design tools often have restrictions on how the FOM can be defined and how many different scenarios can be optimized. They are also often targeted at specific materials or

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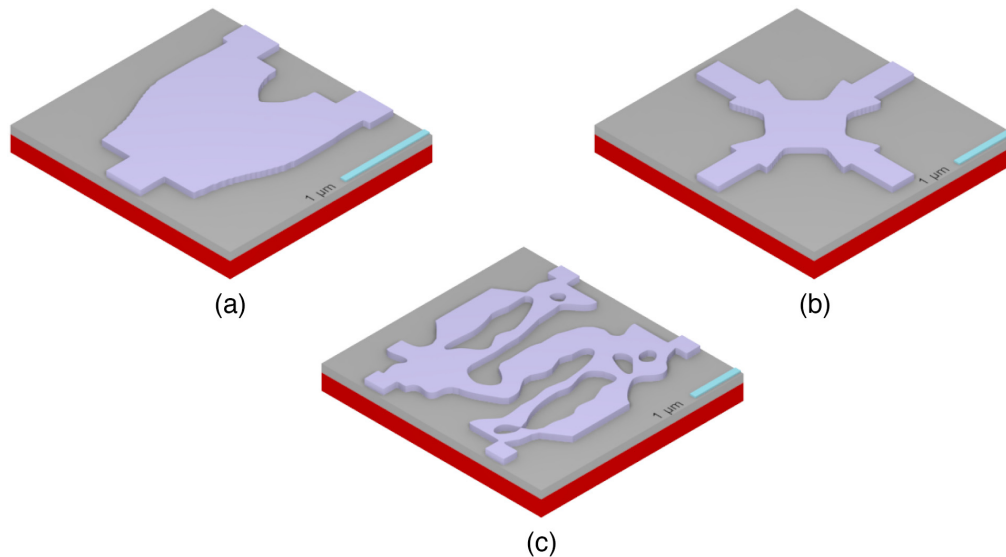


Fig. 1 3D renderings of the inverse-designed optimized devices: (a) y-splitter, (b) waveguide crossing, and (c) XOR gate. The devices are not set to the same relative scale.

architectures, such as silicon photonics. In addition, although the underlying code implementing the adjoint optimization may be provided (as is the case with Lumerical's tools), this code is often quite long and complicated. In fact, making modifications to the code could in itself constitute a significant undertaking and may be outside the project scope of designers who simply want to leverage inverse design as a tool. This leaves the question of how useful these tools are for solving complex design problems without modifying the source code. Furthermore, even if they can be used for more complex designs, there is a question of what limitations of the tools will be necessary to overcome.

In this work, we leveraged Lumerical's inverse design tool to design a compact plasmonic device with logic-gate behavior that acts on phase-encoded inputs. The device is made using dielectric-loaded surface plasmon polariton (DLSP) waveguides. Both the phase-encoded inputs and the plasmonic nature of the device presented unique challenges for implementing the commercial inverse design tool, which is primarily intended for silicon photonics. We found solutions to implementing the inverse design tool within the tool's normal constraints rather than within the Python code containing the underlying algorithm, modifying only the base simulations, and the accompanying setup script responsible for launching the tools. In addition, we compare the performance of the inverse design tool for designing other common photonic circuit components with the same DLSP waveguide architecture. The inverse-design optimized devices are shown in 3D renderings in Fig. 1.

2 Background

There are many simulation tools available (such as Optiwave¹³ and OmniSim¹⁴) as well as many inverse design tools (such as Spins¹⁵ and TopOpt¹⁶); often, many researchers even create their own inverse-design tools and methods. We considered both simulation method and the packaged inverse design tools before deciding to use Lumerical's inverse design tool, LumOpt. FDFD simulation software is typically restricted to 2D simulations and is better able to handle material dispersion. FDFD methods are useful for small structures that are highly resonant. Finite-element method (FEM) simulations are better for time-harmonic problems and are not as useful in simulating propagating light. The FDTD simulation method, used by Lumerical, Optiwave, and OmniSim, is a very generalized method and can easily handle large, 3D devices. In addition, the use of time when calculating finite-difference equations allows users to observe the fields evolve as a solution is being reached. Based on our desire to create fabricable, nonresonant, 3D devices, inverse design tools using an FDTD solver are preferable.

Inverse design tools tend to operate in a very similar manner to each other, so we evaluated them based on their relative integration with the simulation software. Spins, an inverse design tool created at Stanford, is an open-source tool written in Python integrated with an open-source FDTD solver also developed by the same Stanford group. Although Spins allow users to define their own FOM, an advantage compared to LumOpt, being integrated with an FDTD solver limits its applicability to our goal of designing plasmonic waveguide devices. TopOpt is another inverse design tool that is written in MATLAB and useable with COMSOL. Although TopOpt is popular and has a number of associated applications, COMSOL uses FEM simulations instead of the FDTD method. COMSOL has a beam propagation method module available as well, but this method can struggle with simulating larger devices and TopOpt is only designed to work with FEM simulations. The integration between COMSOL and MATLAB is also limiting, partially due to the complexity of COMSOL and because MATLAB is a separate piece of commercial software which also must be purchased. Therefore, we chose to use Lumerical FDTD in combination with its inverse design package LumOpt as a general-purpose tool which best suits our application.

We focused on plasmonic devices for a number of reasons. An excellent case has been made for the use of plasmonics to act as active elements in a hybrid circuit with silicon photonics acting as passive waveguides in large-scale photonic integrated circuits (PICs).¹⁷ Plasmonic devices offer tight confinement of the optical fields and shorter wavelengths than in fully dielectric waveguides, which allows them to have smaller footprints than their silicon photonic counterparts. They also interface easily with electronic circuits, which is desirable for many active components.¹⁸ We selected a DLSP waveguide architecture [Fig. 2(a)] for its relatively low propagation loss and ease of fabrication.¹⁹ The architecture consists of a 500-nm layer of silver on a silicon substrate with a patterned dielectric layer on top of that. We used SiO₂ for the dielectric layer, but other transparent dielectrics, such as optical polymers, could be used as well.^{20,21}

An important application of photonic logic devices is for use in basic processing and routing in fiber-optic communication networks.^{18,22} Many of these networks take advantage of dense encoding schemes for transmission, such as quadrature amplitude modulation or phase-shift keying (PSK). However, dense encoding schemes typically have to be translated to a normal binary encoding when processing information electronically. Designing photonic devices that operate on denser encoding schemes would preclude that requirement, saving power, and increasing throughput.²³ For optical processing, PSK encoding schemes are preferable to other, denser options, because PSK has continuous, uniform, and unambiguous transitions between encoded states. Therefore, we choose to design our devices to operate on a binary PSK (BPSK) encoding scheme, where two different phase states of the signal represent digital 0 and digital 1 [Fig. 2(b)].

The goal of this work was to use inverse design tools to implement digital logic with photonic devices. Although inverse design has been shown for nonlinear devices,⁸ the Lumerical inverse design tools only work for linear designs.²⁴ Although linear device designs using interference have shown logic function behavior with amplitude-encoded inputs, nonlinear optical processes

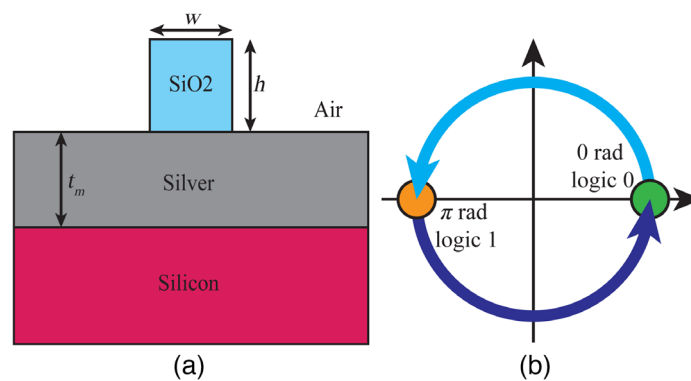


Fig. 2 (a) Cross-section of the single-mode waveguide portion of the devices being simulated, where $w = 400$ nm, $h = 440$ nm, and $t_m = 500$ nm. (b) Binary PSK diagram. A relative phase of 0 radians corresponds to a logic 0, and π radians corresponds to a logic 1.

Table 1 XOR device truth table.

A (rad)	B (rad)	XOR	XNOR
0/0	0/0	0/OFF	1/ON
0/0	$1/\pi$	1/ON	0/OFF
$1/\pi$	0/0	1/ON	0/OFF
$1/\pi$	$1/\pi$	0/OFF	1/ON

are required to achieve most logic functions with phase-encoded inputs. An exception to this is the XOR gate,²⁵ which can be demonstrated with linear functions. XOR logic gates are useful for a number of computing applications, and the typical behavior of a two-input XOR gate is that the output is true (1) when the inputs are different from each other and false (0) otherwise. This behavior, as it was implemented in our devices with PSK encoded inputs and amplitude encoded outputs, is represented in Table 1. Due to the limitations of inverse design and the usefulness of XOR gates for digital logic, we choose to implement this logic function in our design.

Y-splitters are a commonly used integrated device that take an input signal and split it to two outputs. In a typical design, the input signal passing through the y-splitter is split evenly, causing 50% of the signal's power goes to each output, although this is often tuned for different splitting ratios. Using inverse design and a plasmonic structure, we can create a y-splitter with a small footprint, while keeping plasmonic losses manageable. Minimizing loss is important to a y-splitter design as the signals can already only reach a max of 50% power at the outputs, so further loss can result in signal degradation.

Waveguide crossings are another basic photonic device that allows two optical signals to pass through one another at a junction while minimizing loss caused by the disturbing the waveguide modes due to the crossing. Using inverse design, we can reduce the footprint of the waveguide crossing and also increase the transmitted power of both signals to the output waveguides after the crossing junction compared to a conventional design.

3 Methods

As previously mentioned, we implemented Lumerical's inverse design tool, a Python suite called LumOpt, to achieve our designs. Specifically, we performed topology optimizations. LumOpt leverages the adjoint method for inverse design optimization.²⁶ This method allows the gradient of a design space to be calculated with only two simulations: the normal or forward simulation and the reverse or adjoint simulation. In the adjoint simulation, the location and direction of the light source and output monitor are swapped. The design is optimized using an FOM that matches the light mode somewhere in the device, typically an output port. Optimization of different outputs is also possible by setting up a unique base (input condition) for each FOM.

Inverse design optimizations using LumOpt can take a significant amount of time to complete, even on simulation computers with a large amount of processing power. This is compounded by the fact that we had to use a uniformly spaced mesh for our simulations. The automatically generated nonuniform mesh was smaller than the inverse design topology resolution near the metal interface, so we used a fixed mesh to avoid errors in the gradient calculation step. Unfortunately, this uniform mesh increased the time to complete simulations.

To speed up the overall design process for the XOR gate, we first optimized the design using 2D simulations. This allowed us to run each individual simulation faster and therefore have a larger number of simulations run, resulting in a better optimization. However, the 2D designs are not as accurate as 3D designs, since they assume infinite extent in the dimension not simulated. This problem is made worse by the fact that we used plasmonic devices, and the plasmonic confinement was in the dimension not simulated. Therefore, 3D optimization is necessary.

After running the 2D optimization, we used the results as the starting point of the 3D optimization. This allowed the optimization to converge more quickly, requiring fewer rounds of

optimization and therefore fewer simulations and less time overall. We also found that the results were better when we optimized with the 2D results as the starting condition as opposed to the default starting condition for optimizations, which is the optimization region having a refractive index halfway between the waveguide index and background index.

The design we optimized had two input waveguides 400-nm wide and spaced $2.5 \mu\text{m}$ apart. The optimization region was $3.5 \mu\text{m} \times 3.5 \mu\text{m}$, and we set the radius filter of the inverse design tool to 200 nm. The radius filter is used for optimizing at the end of the design process to ensure that all features have the specified minimum radius which in turn ensures they are manufacturable. The design had two output waveguides that were also spaced $2.5 \mu\text{m}$ apart and were 400-nm wide.

The inverse design tool has some important limitations that we had to accommodate to realize our goal. First, the adjoint method is implemented in Lumerical such that each base simulation must use only one input light source. Having only one source is an obvious problem for designing a two-input logic gate, which requires two inputs that vary relative to one another. We overcame this limitation using a single source object in Lumerical and selecting symmetric and antisymmetric coupled modes for the inputs of different base conditions which are then co-optimized (Fig. 3). These two cases represent inputs that are in-phase with each other and π radians out of phase with each other, which are suitable for the two conditions we need to define XOR behavior if we are using a BPSK encoding. In order to validate this approach, we reran the simulation with two separate single-mode sources after the optimization was completed to verify it had the same behavior as with the single coupled-mode source used for the optimization. Although we can design with BPSK encoded inputs, we are unable to have higher degrees of PSK due to this limitation.

Next, we are unable to directly select for phase of the signal at the output. Ideally, we would select for phase conditions so our device uses BPSK encoding at both input and output ports. Unfortunately, the mode-matching requirement for the FOM means that we can only select for amplitude at the output, as well as mode if we have a multimode waveguide. (In our case, the output ports were single-mode waveguides.) Although it would be possible to use the same trick we used for the inputs, with two outputs that have a coupled mode, the result would be a trivial design. Therefore, the outputs of our XOR device are amplitude encoded, also known as on-off keying. One positive side effect of this is that we are able to implement two output ports: one which acts as an XOR gate and one which acts as its inverse, XNOR.

To fully characterize our inverse-designed XOR device, we also designed a device with the same behavior using more conventional simulation design methods. Specifically, we designed a multimode interferometer (MMI) device based on a design in Ref. 27. These devices are narrow so they support fewer modes than larger MMI devices and have less complex interference

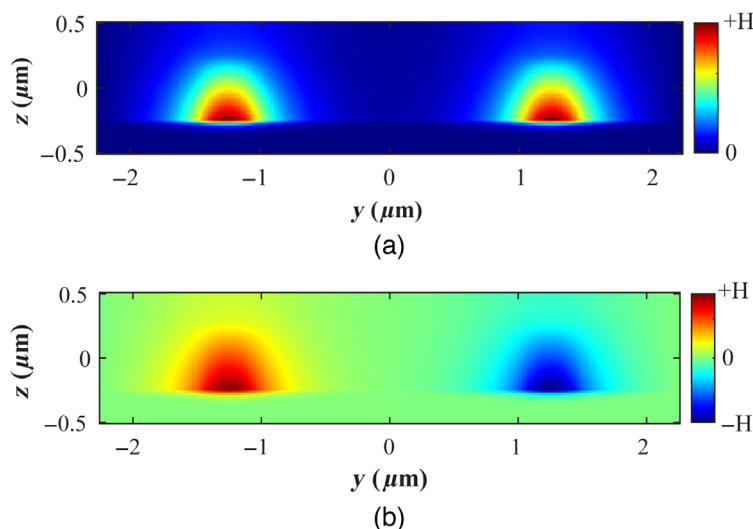


Fig. 3 To simulate different phase relations at the input, we used (a) a symmetric coupled mode for in-phase inputs and (b) an antisymmetric coupled mode for out-of-phase inputs.

patterns.²⁷ On one of the inputs, there is a wide region leading up to the device, which is a phase adjuster. This phase adjuster adds $\pi/2$ radians of phase to that input, which adjusts the interference pattern within the device. This phase adjuster is designed to support the fundamental and first-guided mode and could be redesigned to offer a different phase shift.²⁸ Just as with the inverse-designed device, this conventional device operates with BPSK encoding on the inputs and amplitude encoding on the outputs. One output port acts as an XOR gate, whereas the other acts as an XNOR gate. The size of the input and output waveguides are the same.

For all of our devices, we designed them to operate at a wavelength of 1310 nm, which is a typical communications wavelength. If we want to target other communications wavelengths, the inverse design can easily be rerun to operate at or near a wavelength of 1550 nm, and adjusting the conventional design to operate at or near 1550 nm can also be done as MMIs are well-understood analytically.²⁹

In a similar fashion to the XOR optimization, we used Lumerical and LumOpt to generate an inverse design for a y-splitter. To save computation time, we only simulated a single arm of the y-splitter and then used a symmetric boundary condition to generate the second arm of the device; connecting to the second output waveguide. Due to the symmetry, we use a target FOM of 0.5 at the single output, meaning half of the power of the original signal should reach the output. This results in a symmetric y-splitter structure that has identical outputs to each output waveguide in the device.

The y-splitter inverse design has one input and two output waveguides with the same cross-section dimensions as the XOR device. The output waveguides were spaced $1.4 \mu\text{m}$ away from each other. In addition, the optimization region had a length of $1.8 \mu\text{m}$ and a width of $1.1 \mu\text{m}$, which was located in between the input and top output waveguide, and subsequently mirrored for the lower half of the device, giving an overall device size of $1.8 \mu\text{m} \times 2.2 \mu\text{m}$.

Like the XOR gate, we first ran a 2D simulation to serve as the starting point for the 3D simulation. In the 2D simulation, we specified the initial condition to fill the optimization space with a refractive index halfway between the background and the waveguide indices. Using the 2D results as the initial condition for the 3D optimization, the end results were better than using the other initial conditions.

Unlike the XOR design, there were no major limitations with LumOpt for the y-splitter. We designed a conventional y-splitter using an MMI device as well. The output waveguides were spaced $1.6 \mu\text{m}$ apart, and the MMI region is $2.8 \mu\text{m} \text{ long} \times 2.2 \mu\text{m} \text{ wide}$.

For the waveguide crossing optimization, we again used a co-optimization method to optimize the crossing in both directions simultaneously. The target FOM in each direction is set to 1. Since both source inputs are the same wavelength, we expect a symmetrical design and identical transmission rate for both output waveguides.

The inverse design waveguides use the same cross-section and wavelength as the other designs. The inverse designed crossing had a much smaller footprint at $2.2 \mu\text{m} \times 2.2 \mu\text{m}$, whereas the conventional design had a $3.4 \mu\text{m} \times 3.4 \mu\text{m}$ footprint.

For the waveguide crossing, we only ran the 3D optimization by filling the optimization region halfway between the background and waveguide indices, skipping the initial 2D optimization. We left out the 2D optimization step because the waveguide crossing optimization ran quickly in 3D and gave satisfactory results. Running the 2D optimization first followed by the 3D optimization was overall slower, and the results were similar to optimizing in 3D only. There were no major limitations with LumOpt when designing the waveguide crossing.

The conventional design for the waveguide crossing was also accomplished using overlapping MMI devices in each direction. Each individual MMI region is $3.4 \mu\text{m} \times 1.5 \mu\text{m}$. Using a multimode region, we can reduce the loss and the cross-talk in the region where the waveguides overlap, resulting in better performance than a waveguide crossing of two single-mode waveguides.

4 Results

The topology of the design generated from Lumerical's inverse design tool is shown in Fig. 4(a). The generated design is nonintuitive, but in certain respects is similar to a directional coupler.

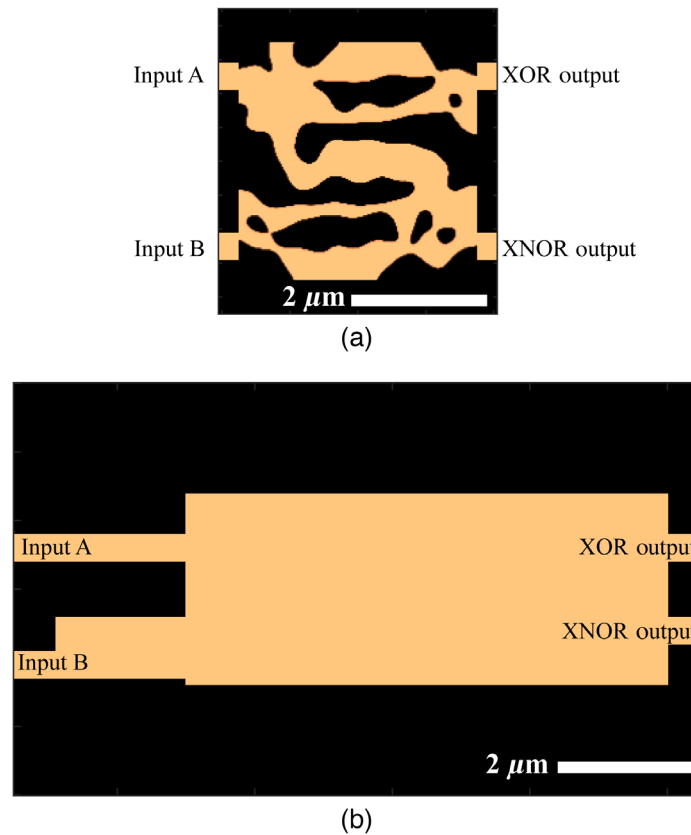


Fig. 4 Topology of XOR devices designed (a) using an inverse-design tool and (b) using conventional methods. The copper color represents the location of SiO_2 . Both diagrams are set to the same scale.

The power inside the device for two different combinations of phase at the input is shown in Figs. 5(a) and 5(b), and the \mathbf{H}_y field is shown in Figs. 5(c) and 5(d), from which you can see the phase relations between the inputs. From these figures, it is plain to see that the inverse-designed device achieves the desired XOR behavior. When the inputs are in phase with one another, the light is directed to the output port on the bottom of the device. Conversely, when the inputs are π radians out of phase with one another, the top output port is selected. These relations translate to an XOR function with phase-encoding on the inputs and amplitude-encoding on the top output port and an XNOR function on the bottom output port.

The topology of the conventionally designed device is shown in Fig. 4(b). The power inside the device and the \mathbf{H}_y fields for different phase combinations at the inputs are shown in Figs. 6(a) and 6(b), and Figs. 6(c) and 6(d), respectively. Once again, these figures demonstrate the desired XOR behavior. This device behaves in the same way as the inverse-designed device. Inputs with signals that are in phase (00 and 11 cases) cause light to couple into the bottom output port, while inputs with signals π radians out of phase with each other (01 and 10 cases) causes light to couple into the top output port.

In addition to confirming the XOR behavior of the inverse- and conventionally designed devices, we characterized their performance. Table 2 compares important metrics between both devices. Specifically, we compared insertion loss, extinction ratio, and device area between both devices. The insertion loss is defined as $\text{loss}(\text{dB}) = -10 \log\left(\frac{P_{\text{out}}}{P_{\text{in}}}\right)$, where P_{out} is the power coupled into the active output port and P_{in} is the input power to the device. The extinction ratio is defined as $\text{ratio}(\text{dB}) = 10 \log\left(\frac{P_{\text{on}}}{P_{\text{off}}}\right)$, where P_{on} is the power coupled into the output port when it is active and P_{off} is the power coupled into the same output port when it is inactive. Finally, the area of the device was calculated as the active area, excluding the input waveguides. For the inverse-designed devices, this area is the area that was topologically inverse designed.

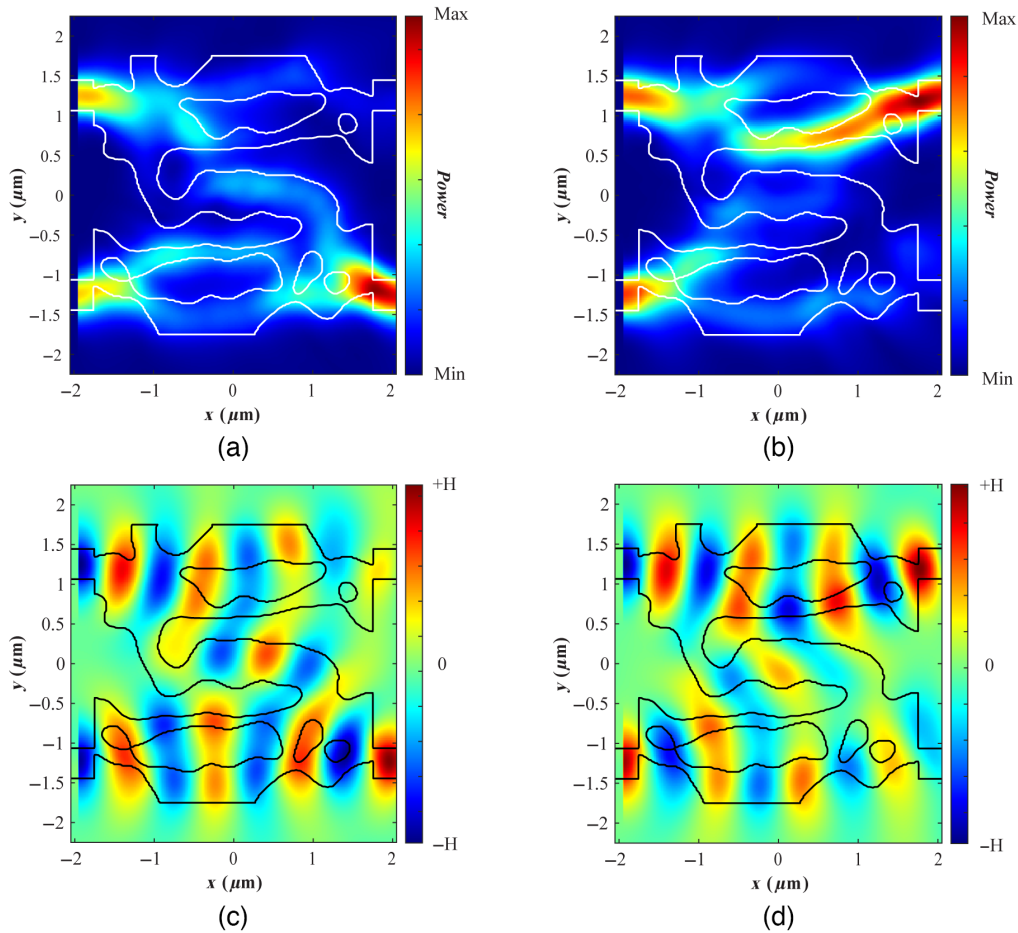


Fig. 5 Simulation results for the inverse-designed XOR device. The top row shows the power in the device when (a) the inputs are in-phase and (b) the inputs are π radians out of phase. The bottom row shows the H_y field, allowing us to view the phase of the signal, when (c) the inputs are in-phase and (d) the inputs are π radians out of phase. The outline in white on plots (a) and (b) and in black on plots (c) and (d) indicates the topology of the device being simulated.

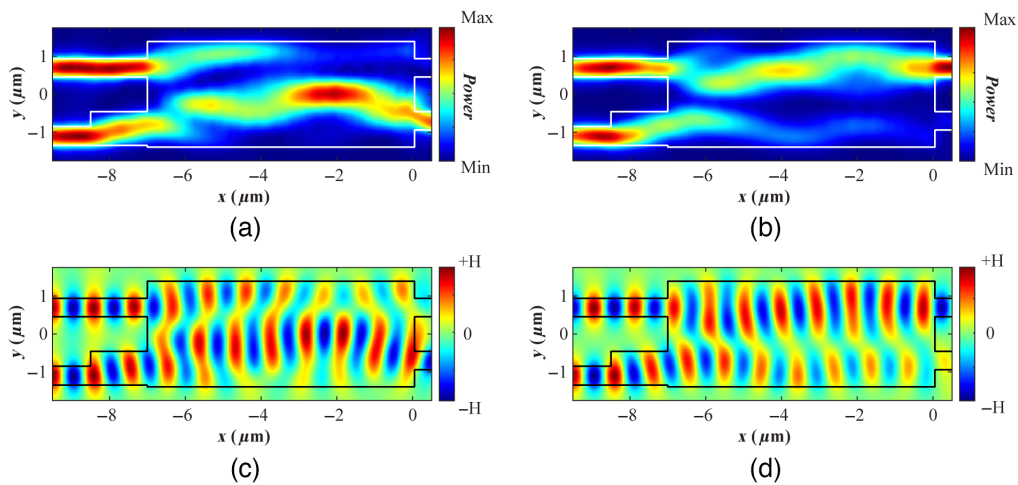


Fig. 6 Simulation results for the conventionally designed XOR device. The top row shows the power in the device when (a) the inputs are in-phase and (b) the inputs are π radians out of phase. The bottom row shows the H_y field, allowing us to view the phase of the signal, when (c) the inputs are in-phase and (d) the inputs are π radians out of phase. The outline in white on plots (a) and (b) and in black on plots (c) and (d) indicates the topology of the device being simulated.

Table 2 XOR gate performance comparison.

Device design	Insertion loss (dB)	Extinction ratio (dB)	Area (μm^2)
Conventional	8.31 (XNOR)/7.38 (XOR)	8.12 (XNOR)/8.49 (XOR)	23.52
Inverse	5.24 (XNOR)/5.5 (XOR)	6.34 (XNOR)/7.28 (XOR)	12.25

The inverse-designed region is $3.5 \mu\text{m} \times 3.5 \mu\text{m}$, which corresponds to an area of $12.25 \mu\text{m}^2$. For the conventionally designed device, we must include the phase adjuster portion, which is essential to achieve the device behavior, so we extended the length to include this component, leading to dimensions of $8.4 \mu\text{m} \times 2.8 \mu\text{m}$. Though this device is narrower than the inverse-designed device, the area is $23.52 \mu\text{m}^2$, which is almost twice the area.

The topology generated for the y-splitters via inverse design and conventional design are shown in Figs. 7(a) and 7(b), respectively. The power inside the device for both devices is depicted in Figs. 8(a) and 8(b). We compare our designs by calculating the splitting ratio, insertion loss, and area. The splitting ratio is defined as $\text{ratio}(\text{top}) = \frac{P_{\text{top}}}{P_{\text{top}} + P_{\text{bottom}}}$ for the top waveguide and $\text{ratio}(\text{bottom}) = \frac{P_{\text{bottom}}}{P_{\text{top}} + P_{\text{bottom}}}$ for the bottom waveguide, where P_{top} and P_{bottom} are the measured output power in each output waveguide. Given our symmetrical design, both splitting ratios at each output should be the same. The insertion loss is calculated in the same way as the XOR gate, using the total power in both arms as the P_{out} .

From this figure, we can see that the inverse designed y-splitter has more power going to each output waveguide than the conventional design. Table 3 compares important metrics between the designs. We calculate that the inverse design has a substantially lower insertion loss, meaning there is less loss overall in the device than in the conventional design. In addition, the inverse design is about a third of the length of the conventional design and a little over half of the width of the conventional design, which leads to a smaller area.

The topologies generated for the waveguide crossings via inverse design and conventional design are shown in Figs. 7(c) and 7(d), respectively. The power inside the device for both devices is shown in Figs. 8(c) and 8(d). We compare the insertion loss, area, and crosstalk of

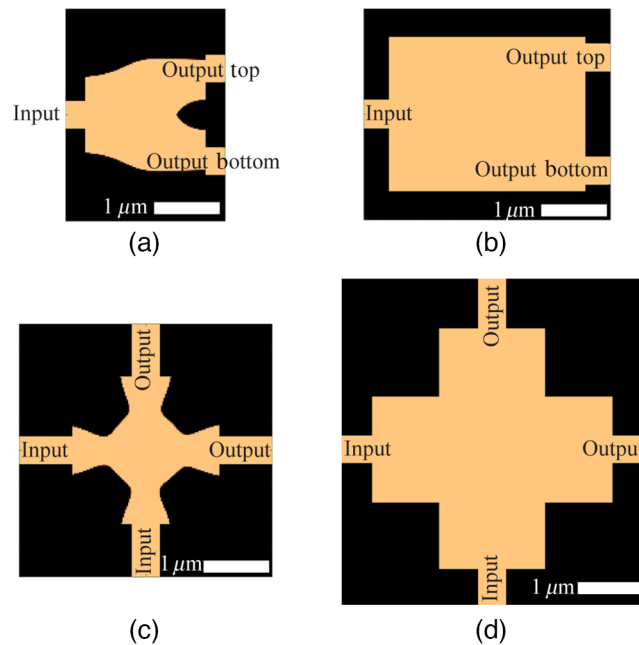


Fig. 7 Topology of designed devices: (a) inverse-designed y-splitter, (b) conventionally designed y-splitter, (c) inverse-designed waveguide crossing, and (d) conventionally designed waveguide crossing. The copper color represents the location of SiO_2 . All diagrams are set to the same scale.

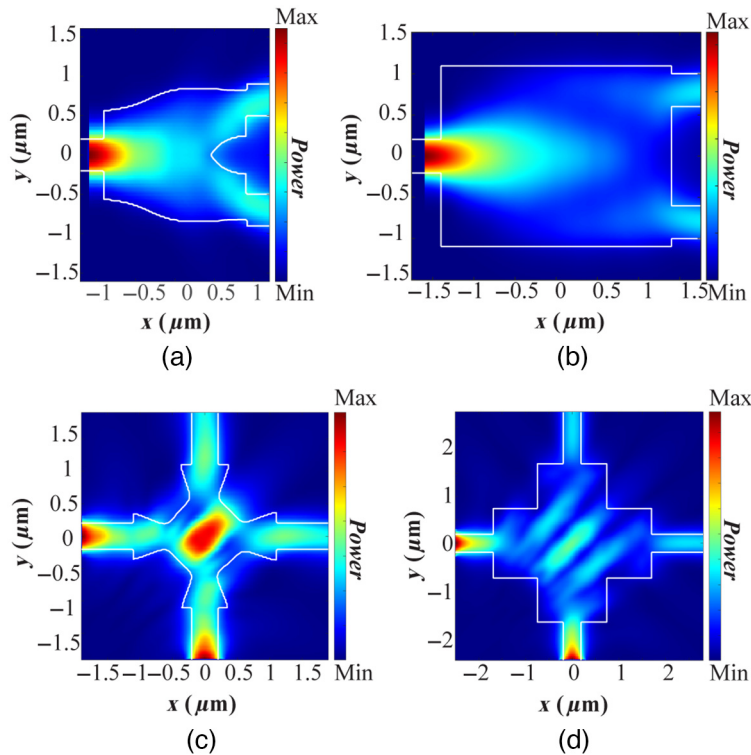


Fig. 8 Simulation results for the power within various devices. (a) Power inside the inverse-designed y-splitter, (b) power inside the conventionally designed y-splitter, (c) power inside the inverse-designed waveguide crossing, and (d) power inside the conventionally designed waveguide crossing. Devices are not to scale. The outlines in white indicate the topology of the device being simulated.

Table 3 Y-splitter performance comparison.

Device design	Insertion loss (dB)	Splitting ratio	Area (μm^2)
Conventional	1.32	50/50	6.16
Inverse	0.696	50/50	3.96

both waveguide crossing designs. The insertion loss for the waveguide crossing is considered for each direction independently and is calculated as in the other devices. The crosstalk is defined as $k(\text{dB}) = 10 \log\left(\frac{P_{\text{cross}}}{P_{\text{through}}}\right)$, where P_{cross} is the output power in the waveguide ports perpendicular to the input and P_{through} is the output power in the desired port.

Table 4 compares important metrics between both devices. The inverse designed waveguide crossing has only slightly lower insertion loss but a much lower overall area compared to the conventional design. In addition, the inverse design has a substantially lower crosstalk.

Table 4 Waveguide crossing performance comparison.

Device design	Insertion loss (dB)	Crosstalk (dB)	Area (μm^2)
Conventional	3.91	-11.8	11.56
Inverse	3.70	-18.4	4.84

5 Discussion

5.1 Evaluating Performance of Design Methods

For all of our designs, the performance of inverse-designed and conventionally designed devices is good for a plasmonic device. The insertion loss of these devices is at an acceptable level, and device-specific metrics are also acceptable. For example, in the XOR gate, both devices show a very good extinction ratio, meaning there is little ambiguity in the device behavior. Finally, all designs have a reasonably small overall area for that type of device, a benefit conferred using plasmonic waveguides.

More interesting features emerge when directly comparing the two design methods for any of the devices. First, the inverse-designed devices generally have a substantially lower insertion loss than the conventionally designed devices. An exception is the waveguide crossing, where the loss is comparable, but the area is significantly smaller and the crosstalk is substantially reduced for the inverse design. The lower insertion loss is primarily due to the reduced propagation distance in the inverse-designed device. Because propagation losses tend to be high in plasmonic devices, a significant improvement is made by reducing the length of the device.

In the XOR gate device, the lower insertion loss represents a performance trade-off. To achieve a shorter length, the inverse-designed XOR gate must also have a wider area than the conventionally designed device. However, this short length probably contributes to the inverse-designed device having a lower extinction ratio than the conventionally designed XOR gate. Although the wider size of the inverse-designed XOR gate may limit how closely these devices could be packed into a single PIC, the overall area of the inverse-designed device is much smaller, so the trade-off is worth it. Furthermore, even though the extinction ratio is lower, it is still at an acceptable level. The width increase is not a problem for the y-splitter or waveguiding crossing devices. Overall, the inverse-designed devices show improved characteristics over the conventionally designed devices.

5.2 Limitations of Inverse Design Tools

For the y-splitter and waveguide crossing designs, there were no significant limitations of the inverse design tool in executing the design. Although the insertion loss did not substantially improve for the inverse-designed waveguide crossing, this is probably more due to the nature of the device itself than a limitation of the tool and is offset by the substantially lower cross-talk. In contrast, despite the good performance of the inverse-designed XOR gate, there are several drawbacks that arose from limitations in the inverse design tool used. The largest drawback is that we are unable to design the XOR device to have a phase-encoded output using Lumerical's inverse design tools. There is no way to use phase of the light at the output port as a design parameter or FOM. To be clear, designing for phase-encoded outputs is a difficult challenge regardless of the tools used. It is desirable to have phase-encoded outputs to enable arbitrary cascading from outputs to inputs of PSK logic devices. However, if we wish to pursue this approach further, we will either need a second stage to the device that re-encodes the output in phase or need to use a different design approach.

Another drawback arises from the limitation that we can only have one input source. Ideally, we would like to design devices that use higher-order PSK, which uses more phase states to represent encoded multibit symbols as opposed to single bits. With one input source, we can represent BPSK inputs by cleverly adapting coupled modes, but this is not possible for higher-order PSK signals. Therefore, to pursue higher-order PSK logic, we will need to use conventional design methods. It is worth noting that higher-order PSK would no longer use binary logic and therefore would require different kinds of logic gates (e.g., a MIN and MAX function) or a translation to binary logic with decoder and encoder gates.³⁰ These are challenging problems worthy of further investigation, and inverse design tools may yet play a role in designing devices for some intermediate stages.

Finally, the Lumerical inverse design tool only works for linear designs. Although this allows us to achieve XOR behavior, if we use phase-encoding, we will need to leverage nonlinear optical effects for other logic functions, which are inherently nonlinear. There are several avenues to

achieve the desired behavior which are currently under investigation, but none of them involve using Lumerical's inverse design tool. Once again, it may be possible that intermediate stages or subcomponents could be designed using these inverse design tools, but it will not be possible to generate a complete device using only inverse design.

6 Conclusion

We used Lumerical's inverse design tool with FDTD simulations to design several plasmonic devices, including an XOR gate, y-splitter, and waveguide crossing. The XOR device has phase-encoded inputs and amplitude-encoded outputs, operating with BPSK. Some of the major design decisions were constrained due to limitations of the inverse design tool being used. To evaluate the performance of the devices and the benefits of using inverse design, we designed plasmonic devices with comparable operation using conventional simulation methods.

Comparing the performance of the inverse-designed devices to the conventionally designed devices illustrates that inverse design provides an improvement in insertion loss and device area. For certain devices, such as the waveguide crossing, device area is much more improved than insertion loss. Other device-dependent metrics, such as extinction ratio for the XOR gate, reveal comparable behavior. These performance improvements highlight the usefulness of inverse design methods for creating novel devices, even when their limitations impose additional design constraints. Moving forward, it is likely that the particular limitations of Lumerical's inverse design tool will prevent it from being used by itself for more complex photonic logic design unless improvements and updates are made. However, this and other inverse design tools may still prove useful for intermediate stages and important subcomponents, such as y-splitters and waveguide crossings. Inverse design tools may help to reduce the overall area and increase the performance of complex, nonlinear, photonic, and plasmonic digital logic devices

Acknowledgments

The authors would like to thank James Kelly of Chapman University for remote management of simulation tools during the COVID-19 pandemic, which enabled this work. This material is based upon work supported by the Air Force Office of Scientific Research (Award No. FA9550-21-1-0188). The authors have no conflicts of interest to disclose.

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